Features

- **Integrated, Industry Standard Enhanced 8051**

- 48 MHz, 24 MHz, or 12 MHz CPU operation
- Four clocks per instruction cycle
- Two USARTS
- Three counter/timers
- Two data pointers
- Expanded interrupt system
- Vectored USB Interrupts and GPIF/FIFO Interrupts

- **Storage**

- 16 Kbytes of On-Chip Code/Data RAM
- 0.5 Kbytes of On-Chip dataRAM

- **Clock, reset**

- 3.3V Operation with 5V Tolerant Inputs
- Power on reset (POR), external RESET input
- 24MHz (± 100ppm) crystal oscillator

- **Low Power**

- It supports suspend mode, and the minimum power consumption is no more than 1mA
- ICC No More than 85 mA in any Mode

- **USB**

- Support standard USB2.0 protocol
- Passed USB2.0 compatibility test of USBIF
- Support high speed mode (480mbps) and full speed mode (12mbps)
- It supports seven endpoints: EP0, ep1in, ep1out, EP2, EP4, ep6 and EP8

- **Integrated FIFO**

- Automatic conversion to and from 16-bit buses
- Master or slave operation
- Synchronous or asynchronous operation
- Easy interface to ASIC and DSP ICs

- **General Programmable Interface (PIF)**

- Enables direct connection to most parallel interfaces
- Support 4 programmable waveform descriptors
- Supports multiple Ready (RDY) inputs and Control (CTL) outputs

- **UART**

- Support 2 UART interfaces
- The maximum baud rate supports 230.4kbaud

- **I2C**

- Operating rate 400kHz or 100kHz
- Only master mode is supported

- **Counter / timer**

- Supports 3 16-bit counters / timers

- **GPIO**

- Up to 5 groups, 40 bidirectional IO in total (only supported by 100pin)

- **Firmware startup**

- Internal RAM, firmware downloaded via USB
- Internal RAM, firmware loaded through EEPROM

- **Package**

- SSOP56：18x7.6x2.8mm
- QFN56：8.0x8.0x1.0mm
- VFBGA56：5.0x5.0x1.0mm
- LQFP100：14x20x1.4mm

- **Operational temperature**

- Operating temperature range (- 40 ~ 105 ℃)

General Description

CBM9002A series is a USB microcontroller based on the enhanced 8051 core in line with the industrial standard. It supports two modes of USB2.0 protocol, high-speed 480mbps and full-speed 12mbps.

The enhanced 8051 can work at 48, 24 and 12Mhz frequencies; Each instruction cycle is 4 clocks, which is 3 times the speed of the standard 8051. CBM9002A series has built-in up to 16K bytes of on-chip SRAM space, which can be used to store user code or data.

CBM9002A series provides USART, I2C, GPIO and other common low-speed communication interfaces other than USB interface for communication with other peripherals.

CBM9002A series supports powerful data transmission functions such as SlaveFIFO and PIF (programmable interface), Based on the CBM9002A series firmware framework provided by CBM, it can achieve data transmission capacity of more than 50MB / s, and the maximum bandwidth is USB2.0.

Application

- Sensor application
- Portable video recorder
- Industrial cameras, or video surveillance equipment
- Data acquisition system
- ATA interface，Such as IDE hard disk
- Memory card readers
- Scanner
- Laser engraving equipment
- Portable sound card or MP3 player
- VGA video capture and transmission equipment, etc

CATALOG

Logic Block Diagram

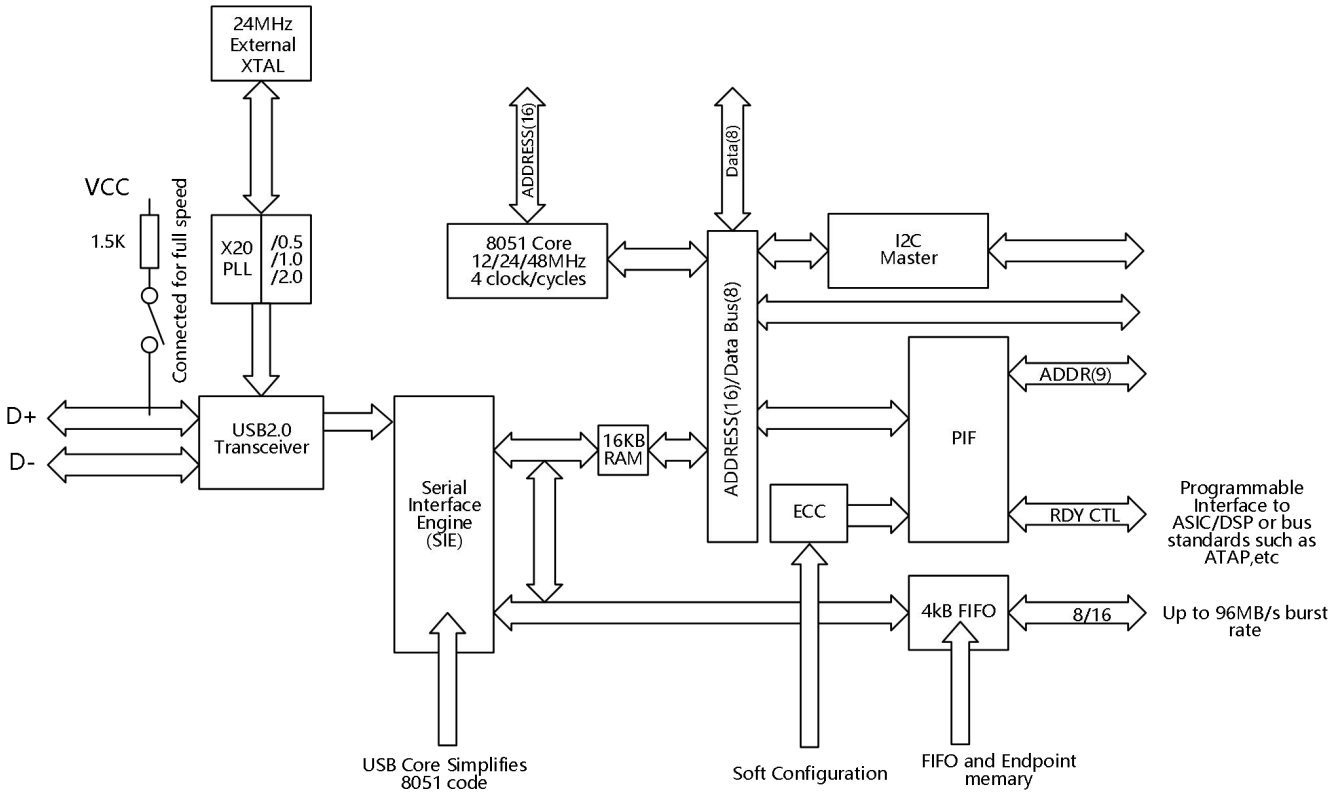


Figure 1. Logic block diagram

Pin assignment

LQFP100 Pin assignment

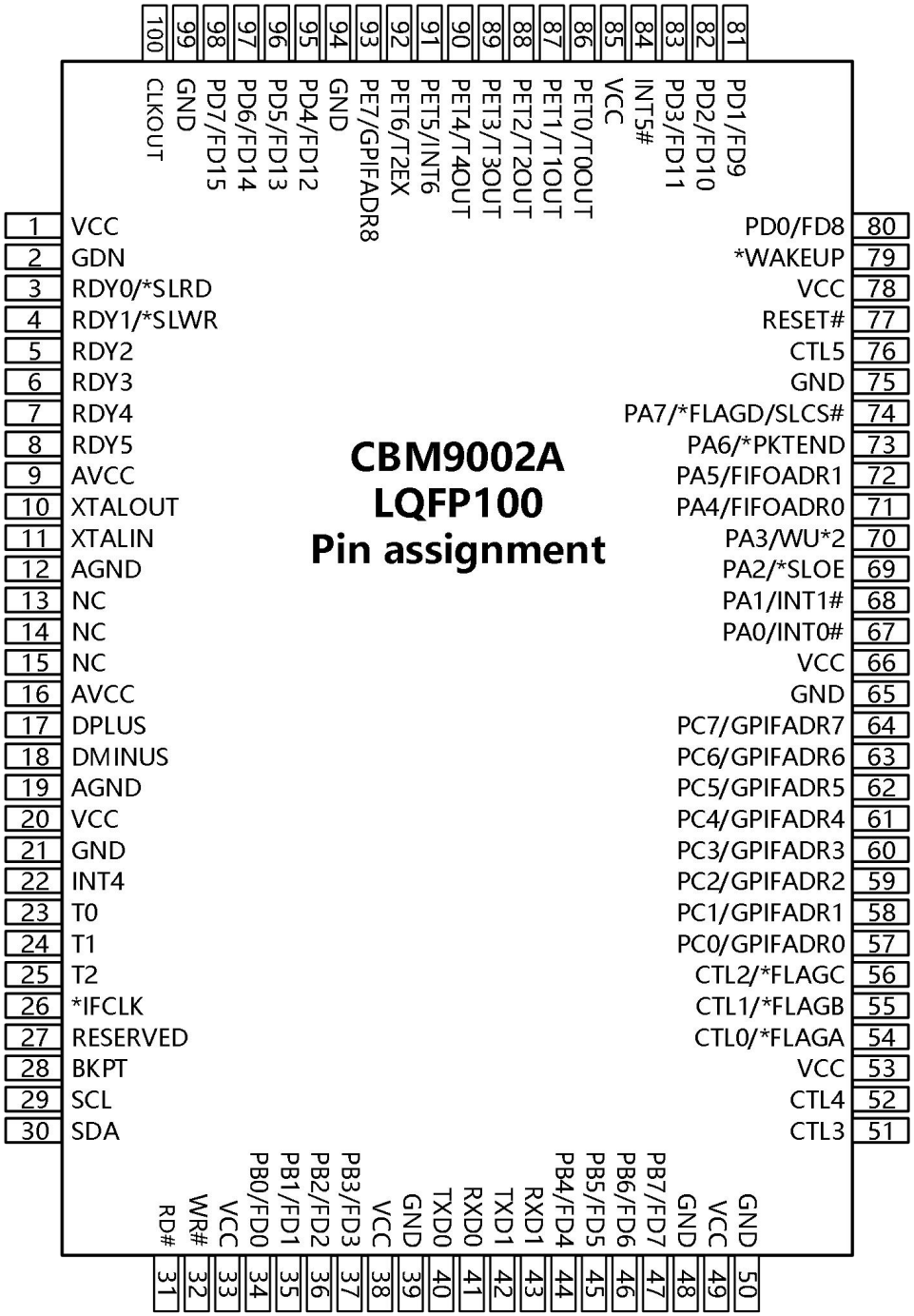


Figure 2. CBM9002A LQFP100 pin assignment

SSOP56 Pin assignment

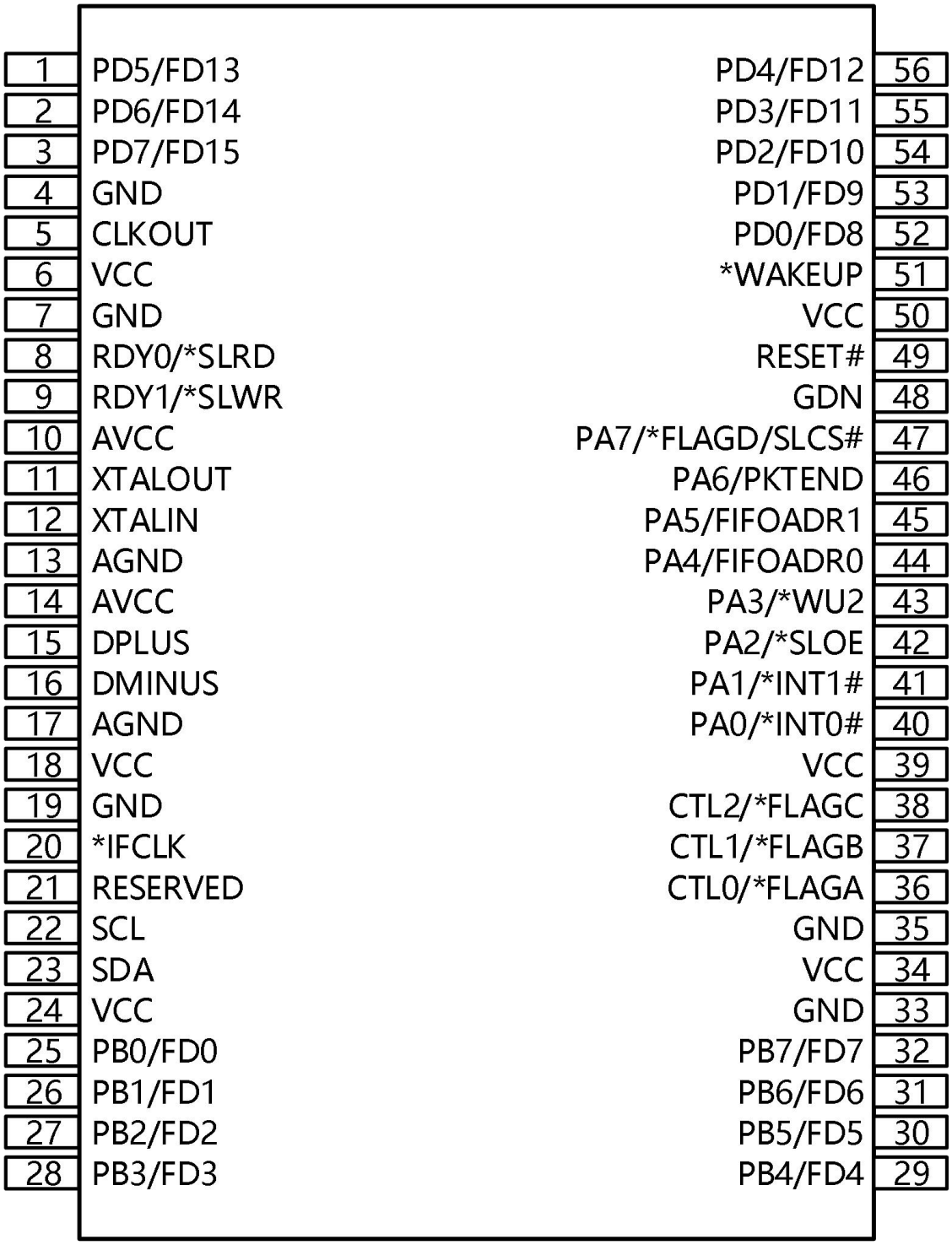


Figure 3. CBM9002A SSOP56 pin assignment

QFN56 Pin assignment

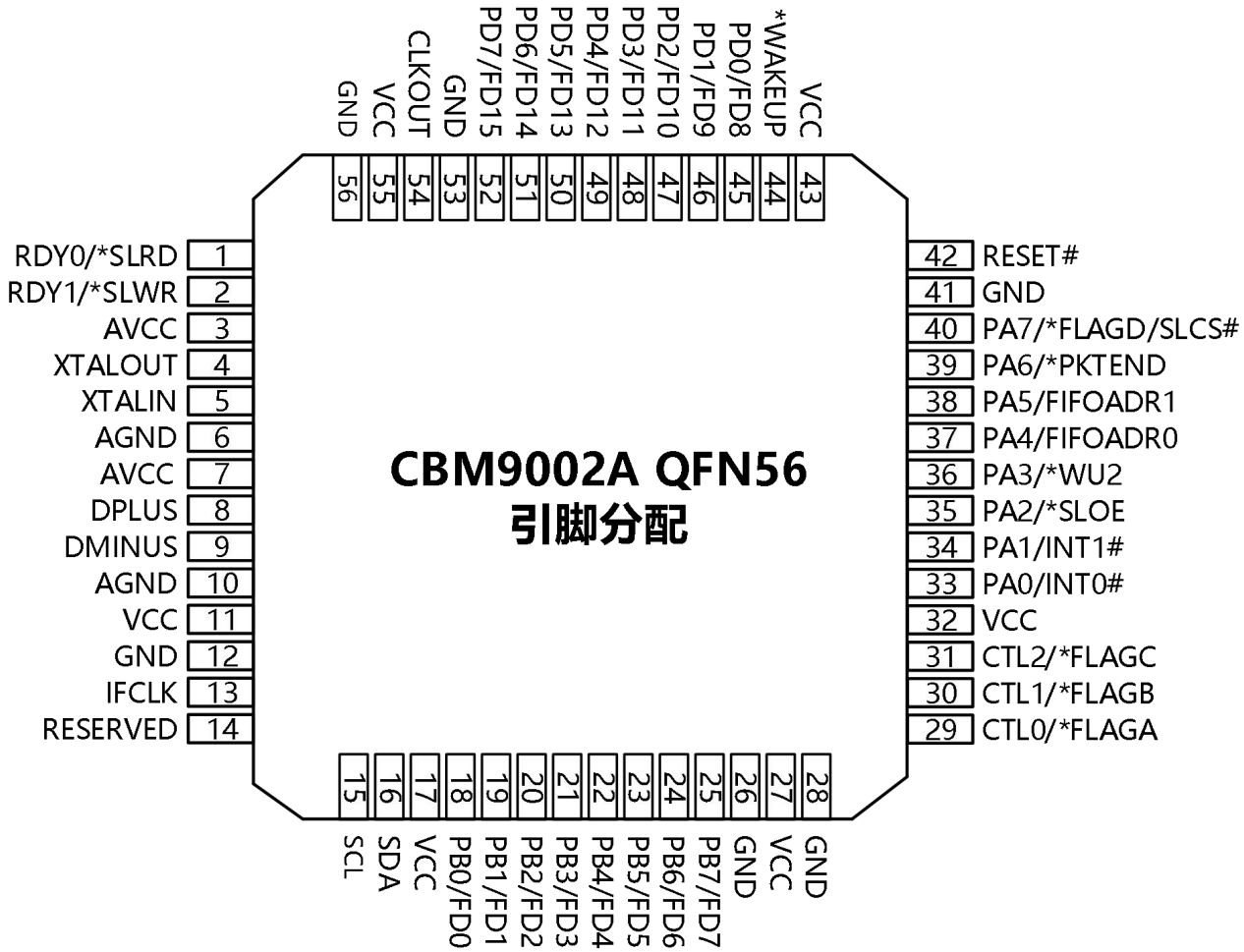


Figure 4. CBM9002A QFN56 pin assignment

VFBGA Pin assignment

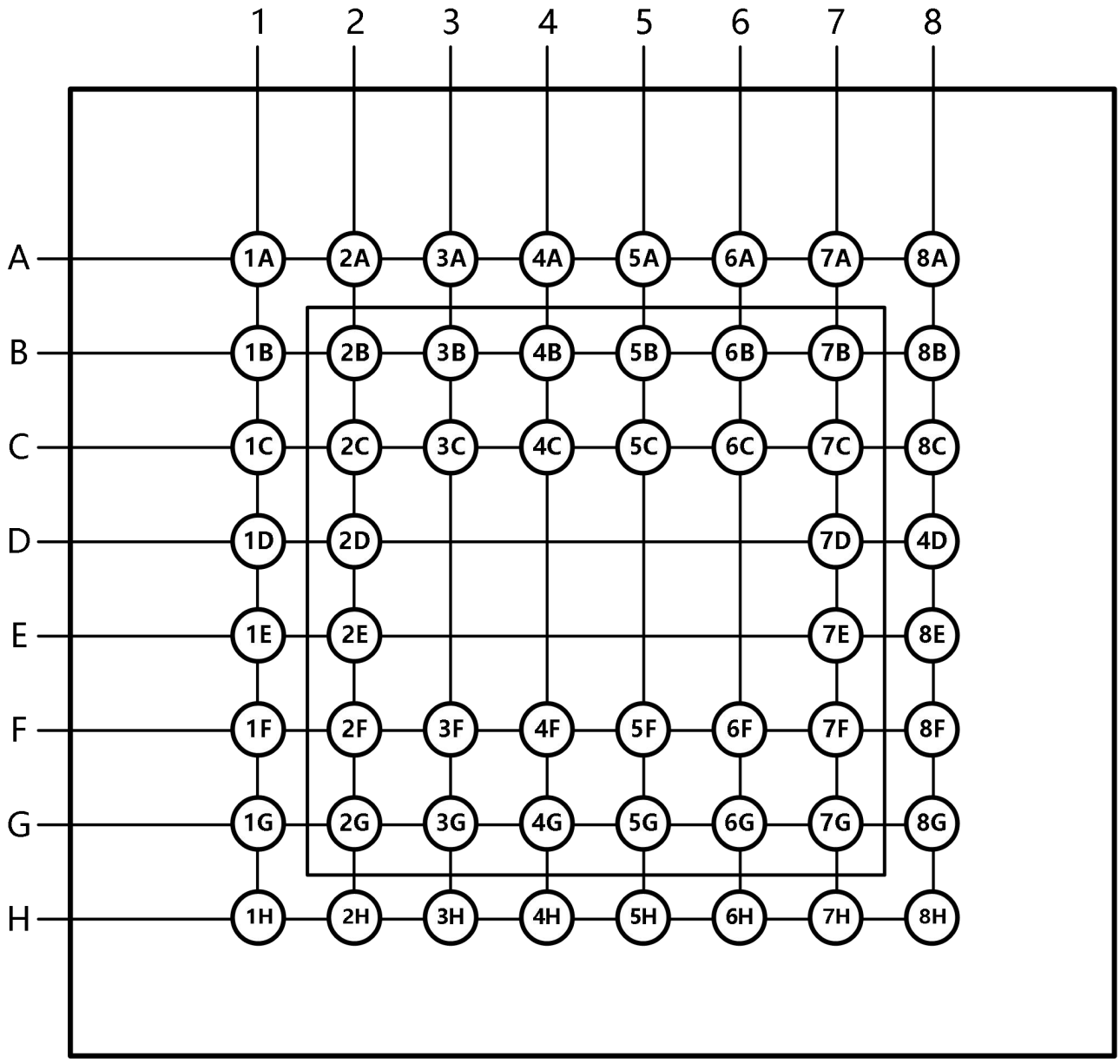


Figure 5. CBM9002A VFBGA pin assignment (Top view)

LQFP-100	SSOP-56	QFN-56	VFBGA-56	名称name	Type	Default	Reset	Notes
9	10	3	2D	AVCC	Power	NA	NA	Analog VCC
16	14	7	1D	AVCC	Power	NA	NA	Analog VCC
12	13	6	2F	AGND	Power	NA	NA	Analog GND
19	17	10	1F	AGND	Power	NA	NA	Analog GND
18	16	9	1E	DMINUS	IO/Z	Z	NA	USBD-Signal
17	15	8	2E	DPLUS	IO/Z	Z	NA	USBD+Signal
28	-	-	-	BKPT	O	L	L	Breakpoint
77	49	42	8B	RESET#	I	NA	NA	Chip reset, low effective
11	12	5	1C	XTALIN	I	NA	NA	24MHz Crystal Input
10	11	4	2C	XTALOUT	O	NA	NA	24MHz Crystal Output
100	5	54	2B	CLKOUT	O/Z	12MHz	Clock drive	12 / 24 / 48mhz clock output, three state output can be set
67	40	33	8G	PA0_INT0#	IOZ	I	I	PA port bit0; Or 8051INT0 interrupt input
68	40	34	6G	PA1_INT1#	IOZ	I	I	PA port bit1; Or 8051INT0 interrupt input
69	42	35	8F	PA2_SLOE	IOZ	I	Z	PA port bit2; Or input / output enable signal in SlaveFIFO mode
70	43	36	7F	PA3_WU2	IOZ	I	Z	PA port bit3; Or USB standby wake-up source
71	44	37	6F	PA4_FIFOADR0	IOZ	I	Z	PA port bit4; Or FIFO address bit0

72	45	38	8C	PA5_FIFOADR1	IOZ	I	Z	PA port bit5; Or FIFO address bit1
73	46	39	7C	PA6_PKEND	IOZ	I	Z	PA port bit6; SlaveFIFO mode multiplexing is the request for early termination of packets. If it is not used, use pull-up or firmware to set it high
74	47	40	6C	PA7_FLAGD_SLCS#	IOZ	I	Z	PA port bit7; Or programmable FIFO flag; Or FIFO chip selection signal
34	25	18	3H	PB0_FD0	IOZ	I	Z	PB port bit0; Or FIFO / PIF data bus bit0
35	26	19	4F	PB1_FD1	IOZ	I	Z	PB port bit1 Or FIFO / PIF data bus bit1
36	27	20	4H	PB2_FD2	IOZ	I	Z	PB port bit2; Or FIFO / PIF data bus bit2
37	28	21	4G	PB3_FD3	IOZ	I	Z	PB port bit3; Or FIFO / PIF data bus bit3
44	29	22	5H	PB4_FD4	IOZ	I	Z	PB port bit4; Or FIFO / PIF data bus bit4
45	30	23	5G	PB5_FD5	IOZ	I	Z	PB port bit5; Or FIFO / PIF data bus bit5
46	31	24	5G	PB6_FD6	IOZ	I	Z	PB port bit6; Or FIFO / PIF data bus bit6
47	32	25	6H	PB7_FD7	IOZ	I	Z	PB port bit7; Or FIFO / PIF data bus bit7
57	-	-	-	PC0_PIFADR0	IOZ	I	Z	PC port bit0; Or PIF address output bit0
58	-	-	-	PC1_PIFADR1	IOZ	I	Z	PC port bit1; Or PIF address output bit1
59	-	-	-	PC2_PIFADR2	IOZ	I	Z	PC port bit2; Or PIF address output bit2
60	-	-	-	PC3_PIFADR3	IOZ	I	Z	PC port bit3; Or PIF address output bit3
61	-	-	-	PC4_PIFADR4	IOZ	I	Z	PC port bit4; Or PIF address output bit4
62	-	-	-	PC5_PIFADR5	IOZ	I	Z	PC port bit5; Or PIF address output bit5
63	-	-	-	PC6_PIFADR6	IOZ	I	Z	PC port bit6; Or PIF address output bit6
64	-	-	-	PC7_PIFADR7	IOZ	I	Z	PC port bit7; Or PIF address output bit7

80	52	45	8A	PD0_FD8	IOZ	I	Z	PB port bit0; Or FIFO / PIF data bus bit8
81	53	46	7A	PD1_FD9	IOZ	I	Z	PB port bit1; Or FIFO / PIF data bus bit9
82	54	47	6B	PD2_FD10	IOZ	I	Z	PB port bit2; Or FIFO / PIF data bus bit10
83	55	48	6A	PD3_FD11	IOZ	I	Z	PB port bit3; Or FIFO / PIF data bus bit11
95	56	49	3B	PD4_FD12	IOZ	I	Z	PB port bit4; Or FIFO / PIF data bus bit12
96	1	50	3A	PD5_FD13	IOZ	I		PB port bit5; Or FIFO / PIF data bus bit13
97	2	51	3C	PD6_FD14	IOZ	I	Z	PB port bit6; Or FIFO / PIF data bus bit14
98	3	52	2A	PD7_FD15	IOZ	I	Z	PB port bit7; Or FIFO / PIF data bus bit15
86	-	-	-	PE0_T0OUT	IOZ	I	Z	PE port bit0; Or 8051 timer 0 overflow output signal
87	-	-	-	PE1_T1OUT	IOZ	I	Z	PE port bit1; Or 8051 timer 1 overflow output signal
88	-	-	-	PE2_T2OUT	IOZ	I	Z	PE port bit2; Or 8051 timer 2 overflow output signal
89	-	-	-	PE3_RXD0OUT	IOZ	I	Z	PE port bit3; Or high effective signal from 8051UART0
90	-	-	-	PE4_RXD1OUT	IOZ	I	Z	PE port bit4; Or high effective signal from 8051UART1
91	-	-	-	PE5_INT6	IOZ	I	Z	PE port bit6; Or 8051 external interrupt input signal
92	-	-	-	PE6_T2EX	IOZ	I	Z	PE port bit6; Or the high effective signal input to 8051 timer 2 is used to overload timer 2. Only when EXEN2 is set to be effective can T2EX be effective
93	-	-	-	PE7_PIFADR8	IOZ	I	Z	PE port bit7; Or PIF address output bit8
3	8	1	1A	RDY0_SLRD	I	NA	NA	PIF mode ready state input 0; Or FIFO mode input read signal
4	9	2	1B	RDY1_SLWR	I	NA	NA	PIF mode ready state input 1; Or FIFO mode input write signal
5	-	-	-	RDY2	I	NA	NA	PIF ready input 2

6	-	-	-	RDY3	I	NA	NA	PIF ready input 3
7	-	-	-	RSY4	I	NA	NA	PIF ready input 4
8	-	-	-	RDY5	I	NA	NA	PIF ready input 5
54	36	29	7H	CTL0_FLAGA	OZ	H	L	PIF control output 0; Or FIFO flag A
55	37	30	7G	CTL1_FLAGB	OZ	H	L	PIF control output 1; Or FIFO flag B
56	38	31	8H	CTL2_FLAGC	OZ	H	L	PIF control output 2; Or FIFO flag C
51	-	-	-	CTL3	OZ	H	L	PIF control output 3
52	-	-	-	CTL4	O	H	L	PIF control output 4
76	-	-	-	CTL5	O	H	L	PIF control output 5
26	20	13	2G	IFCLK	IOZ	Z	Z	Interface clock
22	-	-	-	INT4	I	NA	NA	8051 external interrupt input edge and high effective
84	-	-	-	INT5#	I	NA	NA	8051 external interrupt input edge and low valid
25	-	-	-	T2	I	NA	NA	8051 timer 2 count input
24	-	-	-	T1	I	NA	NA	8051 timer 1 count input
23	-	-	-	T0	I	NA	NA	8051 timer 0 count input
43				RXD1	I	NA	NA	8051 UART1 data input
42	-	-	-	TXD1	O	H	L	8051 UART1 data output
41	-	-	-	RXD0	I	NA	NA	8051 UART0 data input
40	-	-	-	TXD0	O	H	L	8051 UART0 data output
32	-	-	-	WR#	O	H	L	External memory write output signal

31	-	-	-	RD#	O	H	L	External memory read output signal
27	21	14	2H	RESERVED	I	NA	NA	The reserved pin must be connected to GND
79	51	44	7B	WAKEUP	I	NA	NA	USB wake-up input
29	22	15	3F	SCL	OD	Z	Z	I2C interface clock
30	23	16	3G	SDA	OD	Z	Z	I2C interface data
1	6	55	5A	VCC	Power	NA	NA	Digital VCC
20	18	11	1G	VCC	Power	NA	NA	Digital VCC
33	24	17	7E	VCC	Power	NA	NA	Digital VCC
38	-	-	-	VCC	Power	NA	NA	Digital VCC
49	34	27	8E	VCC	Power	NA	NA	Digital VCC
53	-	-	-	VCC	Power	NA	NA	Digital VCC
66	39	32	5C	VCC	Power	NA	NA	Digital VCC
78	50	43	5B	VCC	Power	NA	NA	Digital VCC
85	-	-	-	VCC	Power	NA	NA	Digital VCC
2	7	56	4B	GND	Power	NA	NA	Digital GND
21	19	12	1H	GND	Power	NA	NA	Digital GND
39	-	-	-	GND	Power	NA	NA	Digital GND
48	33	26	7D	GND	Power	NA	NA	Digital GND
50	35	28	8D	GND	Power	NA	NA	Digital GND
65	-	-	-	GND	Power	NA	NA	Digital GND

75	48	41	4C	GND	Power	NA	NA	Digital GND
94	-	-	-	GND	Power	NA	NA	Digital GND
99	4	53	4A	GND	Power	NA	NA	Digital GND
13	-	-	-	NC	NA	NA	NA	Not connected, keep hanging
14				NC	NA	NA	NA	Not connected, keep hanging
15	-	-	-	NC	NA	NA	NA	Not connected, keep hanging

Pin Description

Note：I -- Input; O -- Output; Z -- Tristate; OD -- Open Drain; NA – Not Applicable。

Electrical Characteristics

Symbol	Describe	Min	Max	unit
T_S	Storage temperature	-65	150	℃
T_A	Operating temperature (commercial grade)	0	70	℃
	Operating temperature (industrial grade)	-40	105	℃
VCC	VCC to GND voltage	-0.5	4.0	V
V_{IO}	Any IO input voltage	-0.5	5.25	V
I_{IO}	Maximum output current of any IO		10	mA
ESD	Static discharge voltage	2000		V
PD	Dissipation Power		300	mW

Recommended Operating Conditions

Symbol	Describe	Min	Max	unit
T_A	Operating temperature (commercial grade)	0	70	℃
	Operating temperature (industrial grade)	-40	105	℃
VCC	Supply voltage	3.0	3.6	V
VGND	Ground voltage	0	0	V
FOSC	Crystal oscillator input frequency	24 ± 100ppm，Parallel resonance		MHz

DC parameters

Symbol	Describe	Condition	Min	Typ.	Max	Unit
VCC	Supply voltage	-	3.0	3.3	3.6	V
VCC rise	0-3.3V	-	200	-	-	us
V_{IH}	Input high level voltage	-	2.0	-	5.25	V
V_{IL}	Input low level voltage	-	-0.5	-	0.8	V
I_I	Input leakage current	0<VIN<VCC	-	-	10	uA
V_{OH}	Input high level voltage	VCC=3.3V，I_{OUT}=4mA	2.4	2.95	-	V
V_{OL}	Input low level voltage	VCC=3.3V，I_{SINK}=4mA	-	0.12	0.4	V
I_{SUSP}	Suspended power consumption	VCC=3.3V，USB connect	-	100	1000	uA
I_{CC}	Supply current	VCC=3.3V,8051 running, High speed mode	-	37	44	mA
T_{RESET}	Effective power on reset time	VCC=3.0V	5.0	-	-	ms
	Pin reset after power on		200	-	-	us

AC Parameters t_{IFCLK}

PIF synchronization signal

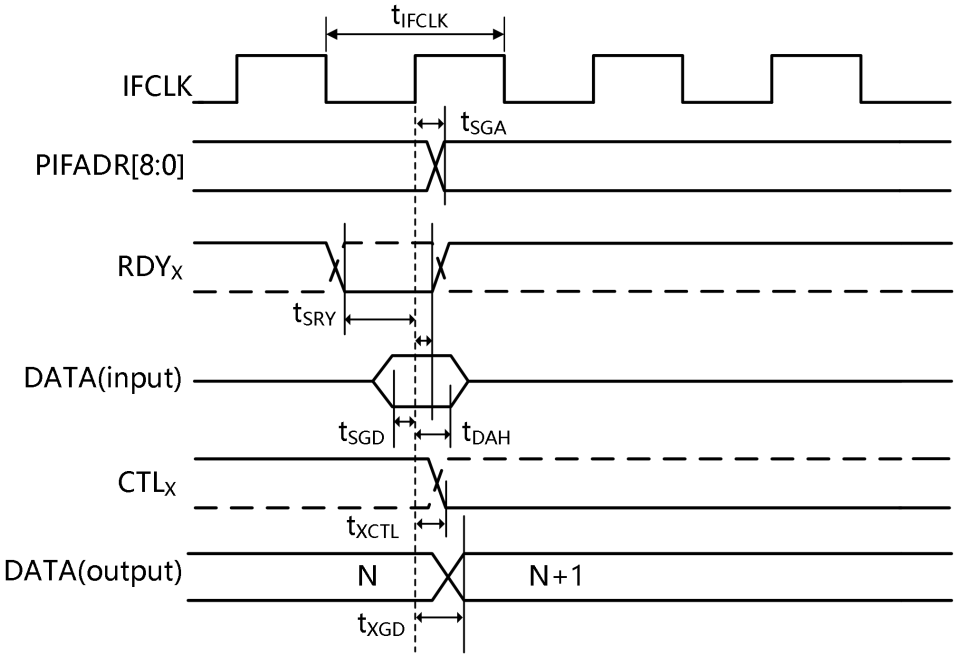


Figure 6. PIF synchronization signal timing diagram

PIF synchronization signal parameters (including internal IFCLK source)

Parameter	Note	Min	Max	Typ		Unit
				Min	Max	
t_{IFCLK}	IFCLK cycle	20.83				ns
t_{SRY}	from RDY_X to clock setup time	8.9				ns
t_{RYH}	From clock setup to RDY_X time	0				ns
t_{SGD}	From PIF data to clock setup time	9.2				ns
t_{DAH}	PIF data retention time	0				ns
t_{SGA}	Transmission delay from clock to PIF address		7.5			ns
t_{XGD}	Transmission delay from clock to PIF data output		10			ns
t_{XCTL}	Transmission delay from clock to CTL_X output		6.7			ns
t_{IFCLKR}	IFCLK rise time				900	ps
t_{IFCLKF}	IFCLK descent time				900	ps
$t_{IFCLKOD}$	IFCLK output duty cycle			49	51	%
t_{IFCLKJ}	IFCLK jitter (peak to peak)				300	ps

PIF synchronization signal parameters (including external IFCLK source)

Parameter	Note	Min	Max	Unit
t_{IFCLK}	IFCLK cycle	20.83	200	ns
t_{SRY}	from RDY_X to clock setup time	2.9		ns
t_{RYH}	From clock setup to RDY_X time	3.7		ns
t_{SGD}	From PIF data to clock setup time	3.2		ns
t_{DAH}	PIF data retention time	4.5		ns
t_{SGA}	Transmission delay from clock to PIF address		11.5	ns
t_{XGD}	Transmission delay from clock to PIF data output		15	ns
t_{XCTL}	Transmission delay from clock to CTL_X output		10.7	ns

Synchronous FIFO read

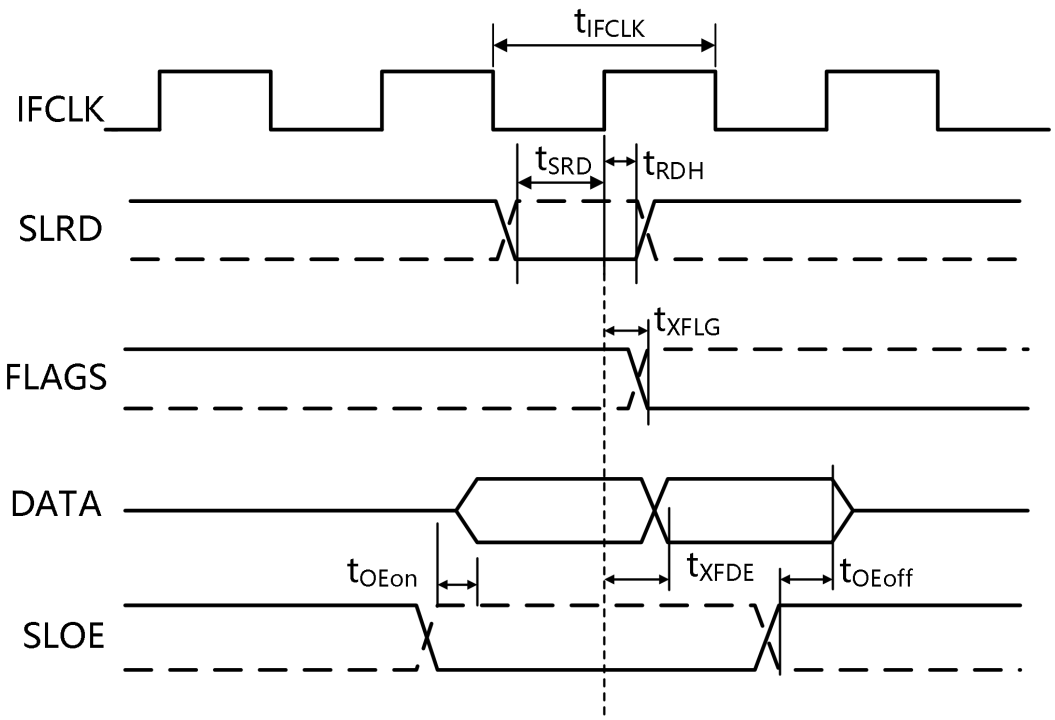


Figure 7. Synchronous FIFO read signal timing

Synchronous FIFO read signal timing (internal IFCLK source)

Parameter	Note	Min	Max	Typ.		Unit
				Min	Max	
t_{IFCLK}	IFCLK cycle	20.83				ns
t_{SRD}	From SLRD to clock setup time	18.7				ns
t_{RDH}	Hold time from clock to SLRD	0				ns
t_{OEon}	From SLOE startup to FIFO data validity			10.5		ns
t_{OEoff}	From XLOE off to FIFO data hold			10.5		ns
t_{XFLG}	Transmission delay from clock to FLAGS output			9.5		ns
t_{XFD}	Transmission delay from clock to FIFO output			11		ns
t_{IFCLKR}	IFCLK rise time				900	ps
t_{IFCLKF}	IFCLK descent time				900	ps
$t_{IFCLKOD}$	IFCLK output duty cycle			49	51	%
t_{IFCLKJ}	IFCLK jitter (peak to peak)				300	ps

Synchronous FIFO read signal timing (external IFCLK source)

parameter	Note	Min	Max	Unit
t_{IFCLK}	IFCLK cycle	20.83	200	ns
t_{SRD}	From SLRD to clock setup time	12.7		ns
t_{RDH}	Hold time from clock to SLRD	3.7		ns
t_{OEon}	From SLOE startup to FIFO data validity		10.5	ns
t_{OEoff}	From SLOE off to FIFO data hold		10.5	ns
t_{XFLG}	Transmission delay from clock to FLAGS output		13.5	ns
t_{XFD}	Transmission delay from clock to FIFO output		15	ns

Synchronous FIFO writes

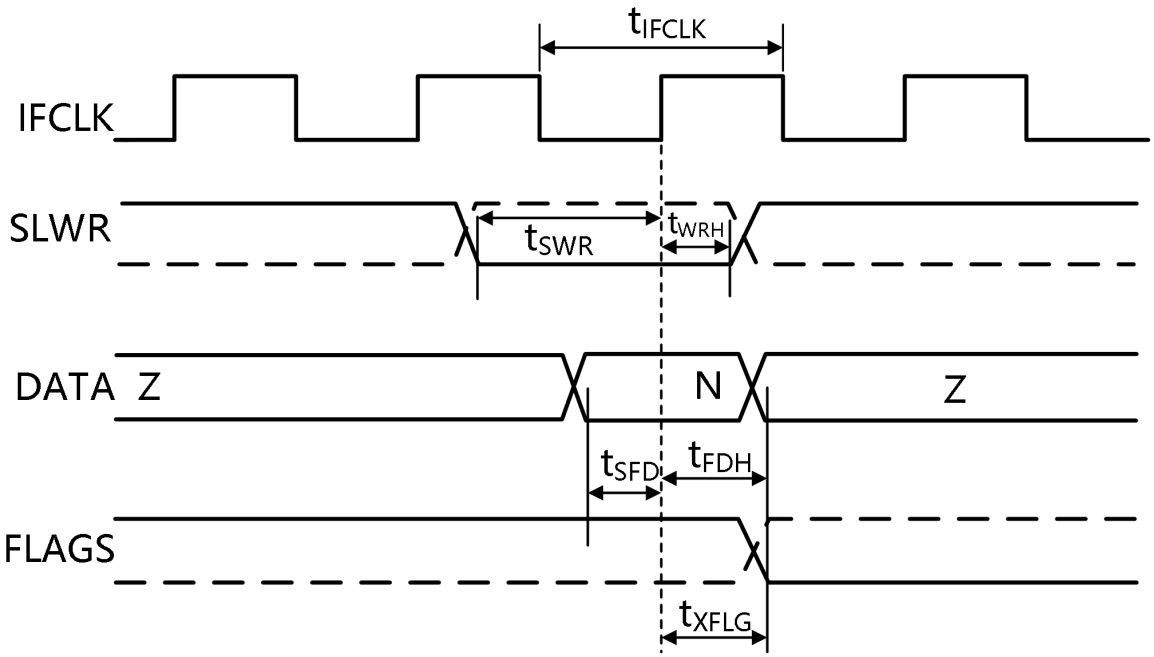


Figure 8. Synchronous FIFO write signal timing

Synchronous FIFO write signal timing (internal IFCLK source)

Parameter	Note	Min	Max	Unit
t_{IFCLK}	IFCLK cycle	20.83		ns
t_{SWR}	Time from SLWR to clock setup	10.4		ns
t_{WRH}	Hold time from clock to SLWR	0		ns
t_{SFD}	Time from FIFO data to clock setup	9.2		ns
t_{FDH}	Hold time from clock to FIFO data	0		ns
t_{XFLG}	Transmission delay from clock to FLAGS output		9.5	ns

Synchronous FIFO write signal timing (external IFCLK source)

Parameter	Note	Min	Max	Unit
t_{IFCLK}	IFCLK cycle	20.83	200	ns
t_{SWR}	Time from SLWR to clock setup	12.1		ns
t_{WRH}	Hold time from clock to SLWR	3.6		ns
t_{SFD}	Time from FIFO data to clock setup	3.2		ns
t_{FDH}	Hold time from clock to FIFO data	4.5		ns
t_{XFLG}	Transmission delay from clock to FLAGS output		13.5	ns

Asynchronous FIFO read

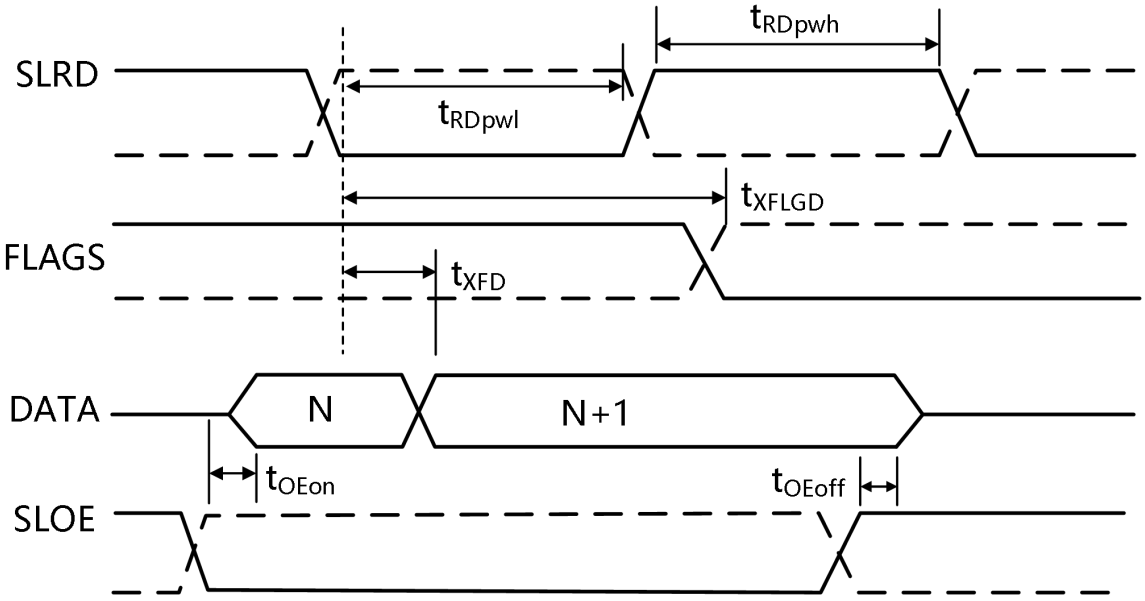


Figure 9. Asynchronous FIFO read signal timing

Asynchronous FIFO read signal timing

Parameter	Note	Min	Max	Unit
t_{RDpwl}	SLRD low pulse width	50		ns
t_{RDpwh}	SLRD high pulse width	50		ns
t_{XFLG}	Transmission delay from SLRD to FLAGS output		70	ns
t_{XFD}	Transmission delay from SLRD to FIFO data output		15	ns
t_{OEon}	From sloe startup to FIFO data validity		10.5	ns
t_{OEoff}	From sloe off to FIFO data hold		10.5	ns

Asynchronous FIFO writes

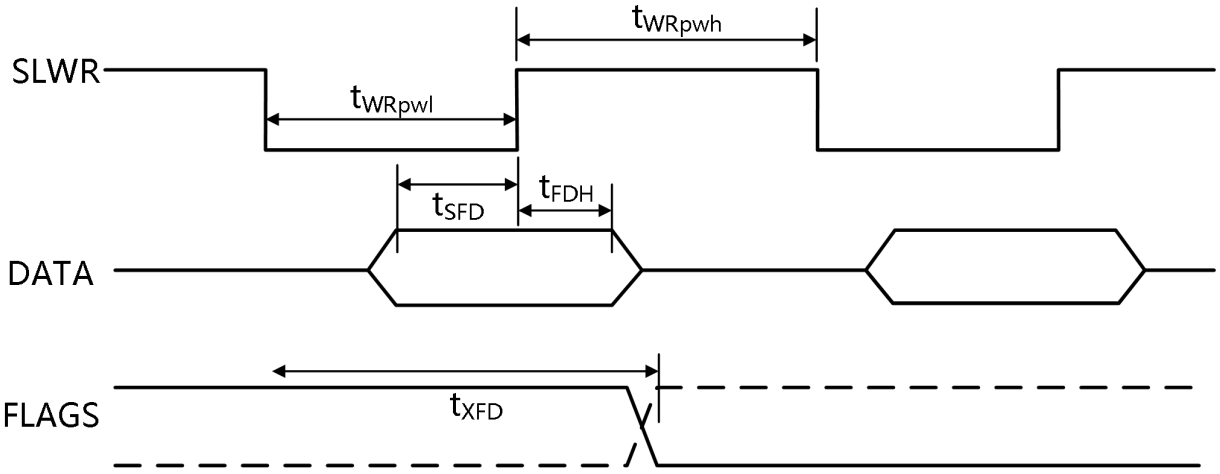


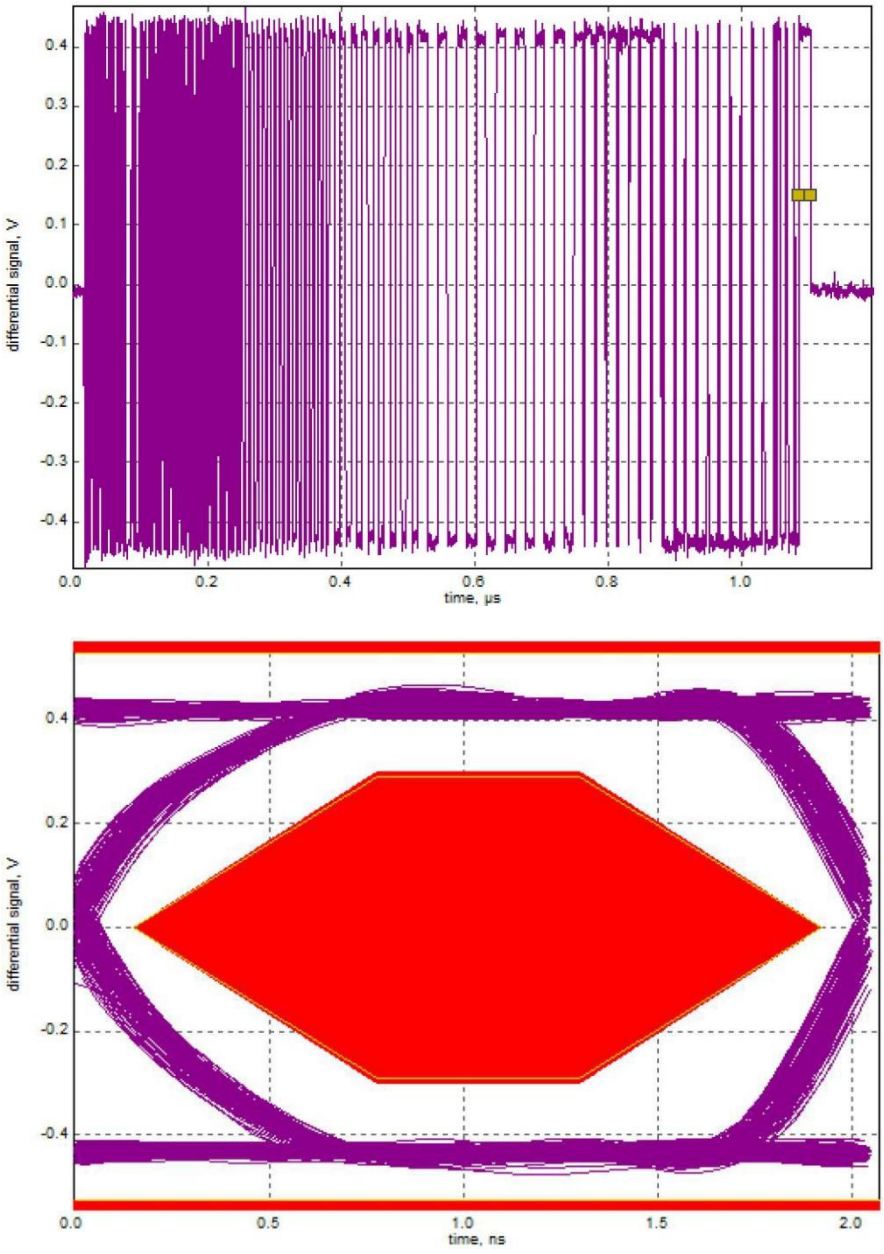
Figure 10. Asynchronous FIFO write signal timing

Asynchronous FIFO write signal timing

parameter	Note	Min	Max	Unit
t_{WRpwl}	SLWD low pulse width	50		ns
t_{WRpwh}	SLWD high pulse width	70		ns
t_{SFD}	Establishment time from SLWR to FIFO DATA	10		ns
t_{FDH}	Hold time from FIFO data to SLWR	10		ns
t_{XFD}	Transmission delay from SLWR to FLAGS output		70	ns

USB Parameter of Consistency

CBM9002A series is fully compatible with USB2.0 protocol standard (except low-speed LS) and USB IF compatibility test standard. The following is the USB2.0 compatibility high-speed eye diagram results obtained based on MSO804A oscilloscope platform of Shide Technology (formerly Agilent Technology) and standard USB2.0 test fixture. The report shows that CBM9002A series has fully passed the compatibility test of USB2.0 high speed (HS480Mbps) and full speed (FS12Mbps).

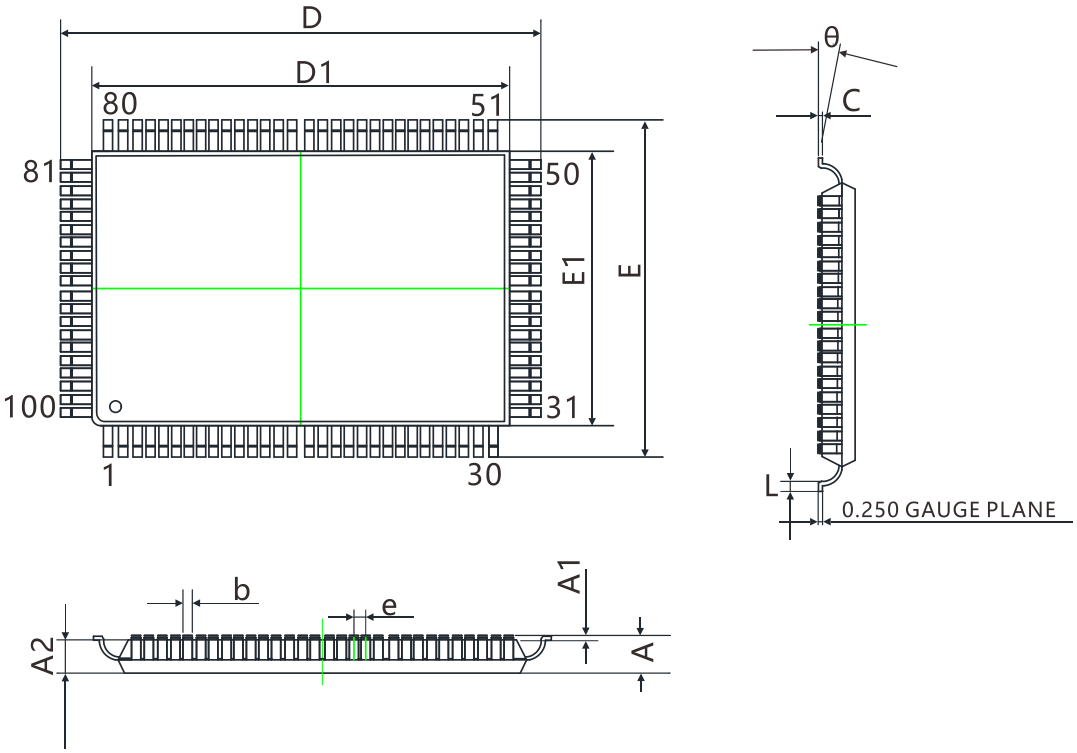


Trial 1: Eye Diagram

Figure 11. Eye diagram results of CBM9002A series USB2.0 high speed compatibility test

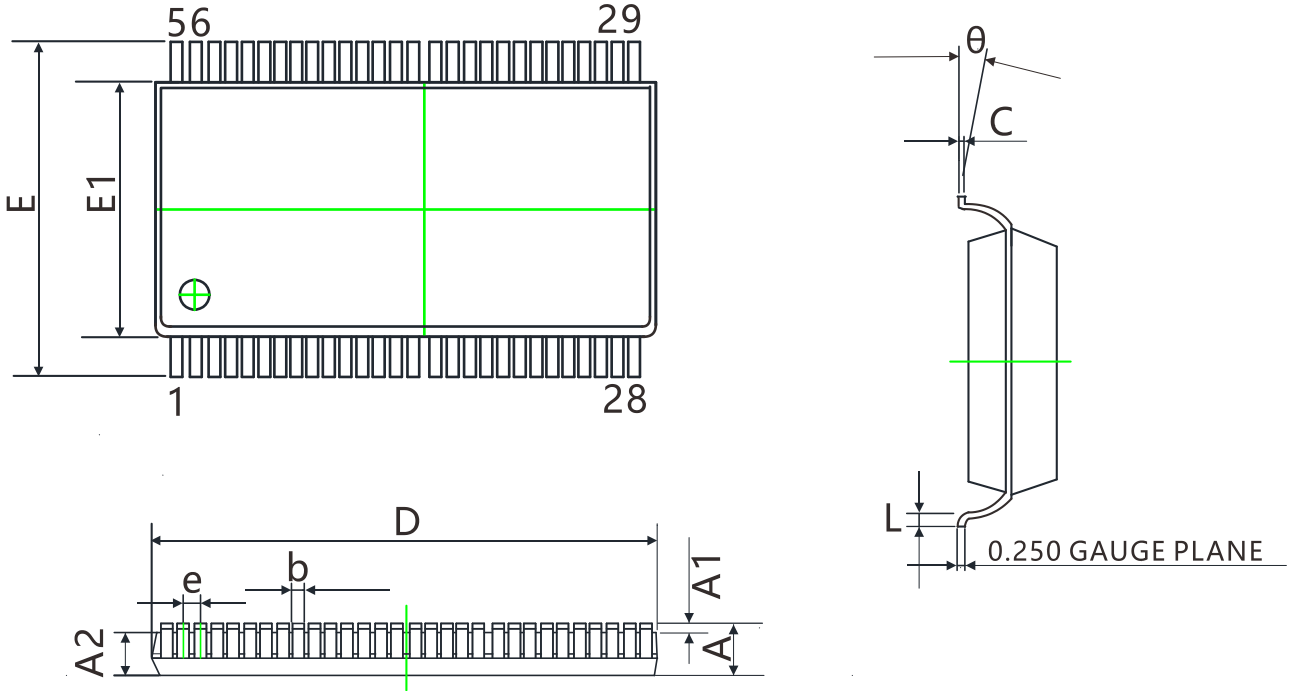
Package Outline Dimensions

LQFP100



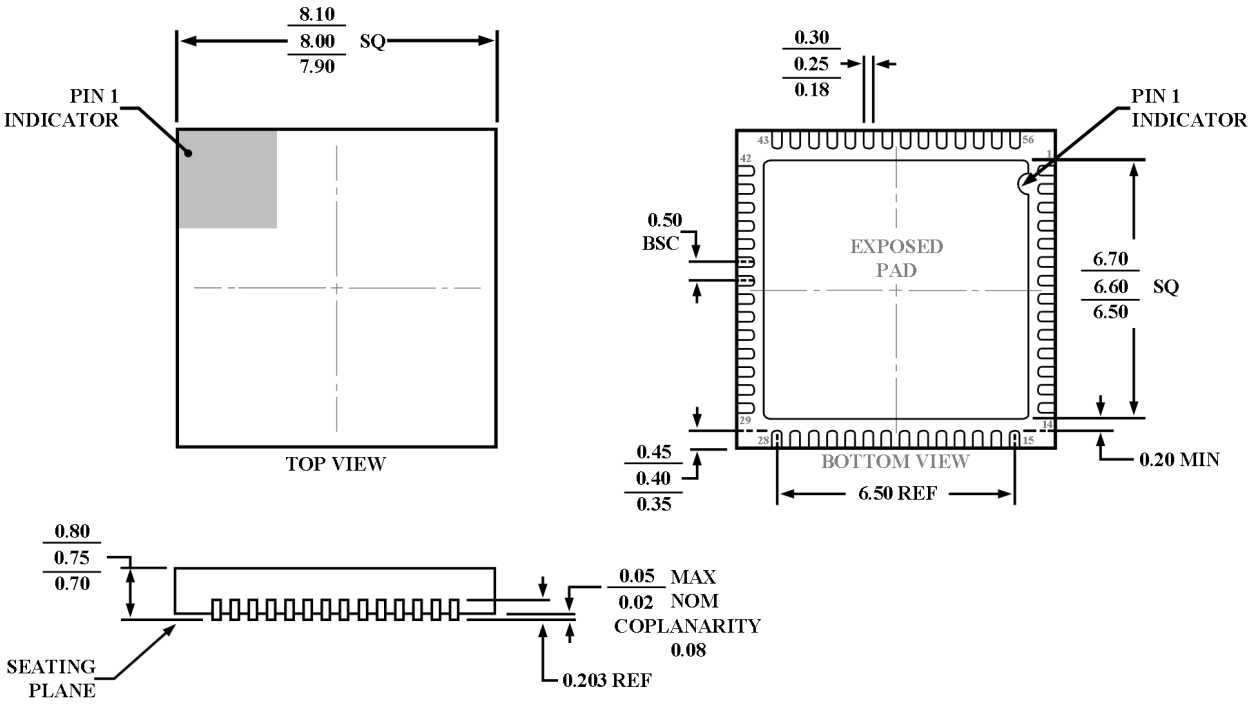
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.600		0.063
A1	0.050	0.150	0.002	0.006
A2	1.350	1.450	0.053	0.057
D	21.80	22.20	0.858	0.874
D1	19.90	20.10	0.783	0.791
E	15.80	16.20	0.622	0.638
E1	13.90	14.10	0.547	0.555
b	0.220	0.380	0.009	0.015
c		0.200		0.008
L	0.450	0.750	0.018	0.030
e	0.650 BSC		0.026 BSC	
θ	0°	7°	0°	7°

SSOP56



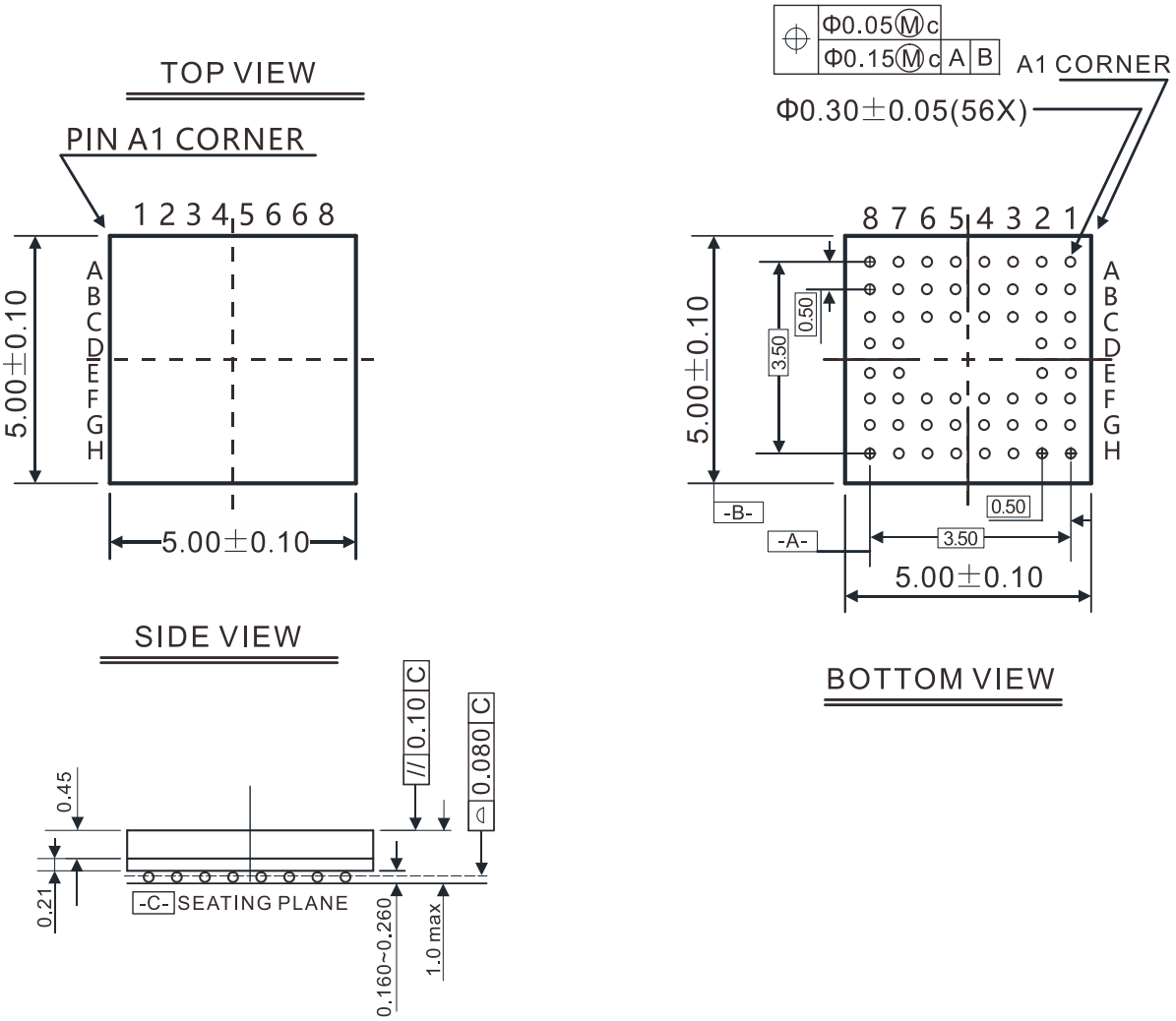
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.438	2.794	0.096	0.110
A1	0.203	0.406	0.008	0.016
A2	2.235	2.337	0.088	0.092
D	18.288	18.542	0.720	0.730
E	10.033	10.668	0.395	0.420
E1	7.417	7.595	0.292	0.299
c	0.127	0.254	0.005	0.010
b	0.203	0.343	0.008	0.014
L	0.610	1.016	0.024	0.040
e	0.635 BSC		0.025 BSC	
θ	0°	8°	0°	8°

QFN56



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
A3	0.203 REF		0.008 REF	
D	7.900	8.100	0.311	0.319
E	7.900	8.100	0.311	0.319
D1	4.400	4.600	0.173	0.181
E1	5.100	5.300	0.201	0.209
b	0.200	0.300	0.008	0.012
e	0.500 BSC		0.020 BSC	
k	1.350 REF		0.053 REF	
k1	1.000 REF		0.039 REF	
L	0.300	0.500	0.012	0.020

VFBGA56


TOP VIEW
PIN A1 CORNER
1 2 3 4 5 6 6 8
A B C D E F G H
5.00±0.10
5.00±0.10
SIDE VIEW
0.45
0.21
-C- SEATING PLANE
0.10 C
0.080 C
0.160~0.260
1.0 max
Φ0.05 M c
Φ0.15 M c A B
A1 CORNER
Φ0.30±0.05(56X)
8 7 6 5 4 3 2 1
A B C D E F G H
5.00±0.10
0.50
3.50
-B-
-A-
0.50
3.50
5.00±0.10
BOTTOM VIEW

Package/Ordering Information

Product	Ordering number	Temperature range	Package description	Making information	Transpot media,quantily
CBM9002	CBM9002A-56ISG	-40℃~105℃	SSOP-56	CBM9002A	Tube,390
	CBM9002A-56SCG	-40℃~105℃	SSOP-56	CBM9002A	Tube,390
CBM9002	CBM9002A-56IBG	-40℃~105℃	BGA-56	CBM9002A	Reel,2500
	CBM9002A-56BCG	-40℃~105℃	BGA-56	CBM9002A	Reel,2500
CBM9002	CBM9002A-56ILG	-40℃~105℃	QFN-56	CBM9002A	Tray,2500
	CBM9002A-56LCG	-40℃~105℃	QFN-56	CBM9002A	Tray,2500
CBM9002	CBM9002A-100TIG	-40℃~105℃	TQFP-100	CBM9002A	Tray,720
	CBM9002A-100TCG	-40℃~105℃	TQFP-100	CBM9002A	Tray,720