Data sheet

BMG250

Low noise, low power triaxial gyroscope

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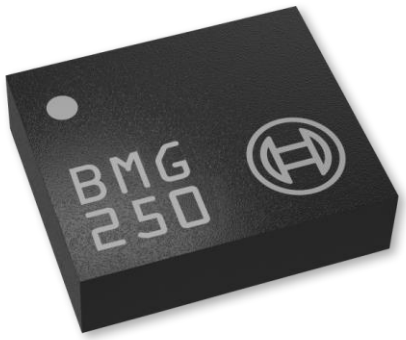

BMG250 – Data sheet

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BMG250
Low noise, low power triaxial gyroscope

The BMG250 is a low noise, low power three axial gyroscope that provides a precise angular rate (gyroscopic) measurement at market leading low power consumption.

The BMG250 is a 16 bit digital, triaxial gyroscope sensor.

Key features

- High performance low noise and low offset gyroscope
- Very low power consumption: typ. 850 µA (gyroscope in full operation)
- Very small 2.5 x 3.0 mm^2 footprint, height 0.83 mm
- Secondary high speed interface for OIS application
    - Optimized for low latency and high Output Data Rate
- Parallel use for OIS and standard UI applications
    - UI → Primary Interface (I^2C)
    - OIS → Secondary Interface (SPI)
- Built-in power management unit (PMU) for advanced power management
- Power saving with fast start-up mode of gyroscope
- Wide power supply range: 1.71V … 3.6V
- Allocatable FIFO buffer of 1024 bytes
- Hardware sensor time-stamps for accurate sensor data fusion
- Flexible digital interface to connect to host over I^2C or SPI
- Extended I^2C mode with clock frequencies up to 1 MHz

Typical applications

- Optical Image Stabilization
- Electronic Image Stabilization
- Optical/Electronic Video Stabilization
- Augmented Reality
- Indoor navigation
- 3D scanning / indoor mapping
- Advanced gesture recognition
- Immersive gaming
- 3-axis motion detection, e.g. Air mouse applications and pointers
- Advanced system power management for mobile applications
- warranty logging

Target Devices

- Smart phones, tablet and transformer PCs
- Camera modules for Smartphones
- Digital Still Cameras / Digital Video Cameras
- Game controllers, remote controls and pointing devices
- Head tracking devices
- Wearable devices, e.g. smart watches or augmented reality glasses
- Sport and fitness devices
- Toys, e.g. toy helicopters

General Description

The BMG250 is a three axial gyroscope consisting of a state-of-the-art low power 3-axis gyroscope. It has been designed for low power, high precision multi-axis applications in mobile phones, tablets, wearable devices, remote controls, game controllers, head-mounted devices and toys. The BMG250 is available in a compact 2.5 × 3.0 × 0.83 mm^3 LGA package. When the gyroscope is in full operation mode, power consumption is typically 850 µA, enabling always-on applications in battery driven devices. The BMG250 offers a wide V_{DD} voltage range from 1.71V to 3.6V and a V_{DDIO} range from 1.2V to 3.6V, allowing the BMG250 to be powered at 1.8V for both V_{DD} and V_{DDIO}.

The BMG250 provides high precision sensor data together with the accurate timing of the corresponding data. The timestamps have a resolution of up to 39 µs.

The integrated 1024 byte FIFO buffer supports low power applications and prevents data loss in non-real-time systems. The intelligent FIFO architecture allows dynamic reallocation of FIFO space. For typical applications, this is sufficient for approx. 1.4s of data capture at an output data rate of 100Hz in FIFO mode with data header.

The smart built-in power management unit (PMU) can be configured, for example, to further lower the power consumption by automatically sending the gyroscope temporarily into fast start-up mode and waking it up again by externally triggering this function from the host device's logical unit.

Besides the flexible primary interface (I^2C or SPI) that is used to connect to the host, BMG250 provides an additional secondary interface. This secondary interface can be used in SPI mode for OIS (optical image stabilization) applications in conjunction with camera modules, or in advanced gaming use cases.

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1. Contents

2. Specification

If not stated otherwise, the given values are over lifetime and full performance temperature and voltage ranges, minimum/maximum values are ±3σ.

2.1 Electrical specification

VDD and VDDIO can be ramped in arbitrary order without causing the device to consume significant currents. The values of the voltage at VDD and the VDDIO pins can be chosen arbitrarily within their respective limits. The device only operates within specifications if the both voltages at VDD and VDDIO pins are within the specified range. The voltage levels at the digital input pins must not fall below GNDIO-0.3V or go above VDDIO+0.3V to prevent excessive current flowing into the respective input pin. BMG250 contains a brownout detector, which ensures integrity of data in the non-volatile memory under all operating conditions.

Table 1: Electrical parameter specification

Operating Conditions BMG250						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Supply Voltage Internal Domains	V_{DD}		1.71	3.0	3.6	V
Supply Voltage I/O Domain	V_{DDIO}		1.2	2.4	3.6	V
Voltage Input Low Level	$V_{IL,a}$	SPI			$0.3V_{DDIO}$	-
Voltage Input High Level	$V_{IH,a}$	SPI	$0.7V_{DDIO}$			-
Voltage Output Low Level	$V_{OL,a}$	V_{DDIO}=1.62V, I_{OL}=3mA, SPI			$0.2V_{DDIO}$	-
		V_{DDIO}=1.2V, I_{OL}=3mA, SPI			$0.23V_{DDIO}$	-
Voltage Output High Level	$V_{OH,a}$	V_{DDIO}=1.62V, I_{OH}=3mA, SPI	$0.8V_{DDIO}$			-
		V_{DDIO}=1.2V, I_{OH}=3mA, SPI	$0.62V_{DDIO}$			-
Operating Temperature	T_A		-40		+85	°C
NVM write-cycles	n_{NVM}	Non-volatile memory	14			Cycles
Current consumption	I_{DD}	Gyro in fast start-up, T_A=25°C		500		µA
		Gyro full operation mode T_A=25°C		850		
		Gyro in suspend mode, T_A=25°C		3		

2.2 Electrical and physical characteristics, measurement performance

Table 3: Electrical characteristics gyroscope

OPERATING CONDITIONS GYROSCOPE						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Range	R_{FS125}	Selectable via serial digital interface		125		°/s
	R_{FS250}			250		°/s
	R_{FS500}			500		°/s
	R_{FS1000}			1,000		°/s
	R_{FS2000}			2,000		°/s
Range (Secondary interface)	R_{FSOIS}	Fixed range setting		2,000		°/s
Start-up time	$t_{G,su}$	Suspend to normal mode ODR_G=1600Hz		55	80	ms
	$t_{G,FS}$	Fast start-up to normal mode		10	15	ms

OUTPUT SIGNAL GYROSCOPE						
Sensitivity	R_{FSOIS}	Ta=25°C	15.9	16.4	16.9	LSB/°/s
	R_{FS2000}	Ta=25°C	15.9	16.4	16.9	LSB/°/s
	R_{FS1000}	Ta=25°C	31.8	32.8	33.8	LSB/°/s
	R_{FS500}	Ta=25°C	63.6	65.6	67.6	LSB/°/s
	R_{FS250}	Ta=25°C	127.2	131.2	135.2	LSB/°/s
	R_{FS125}	Ta=25°C	254.5	262.4	270.3	LSB/°/s
Sensitivity change over temperature	TCS_G	R_{FS2000}, Nominal V_{DD} supplies best fit straight line		±0.02		%/K
Nonlinearity	NL_G	Best fit straight line R_{FS1000}, R_{FS2000}		0.1		%FS
g- Sensitivity		Sensitivity to acceleration stimuli in all three axis (frequency <20kHz)			0.1	°/s/g
Zero-rate offset	Off Ω_x Ω_y and Ω_z	T_A=25°C, fast offset compensation off		±3		°/s
Zero-Rate offset Over temperature	Off $\Omega_{x,oT}$ $\Omega_{y,oT}$ and $\Omega_{z,oT}$	-40°C $\leqslant T_A \leqslant$ +85°C		±3		°/s
Zero-rate offset change over temperature	TCO_G	-40°C $\leqslant T_A \leqslant$ +85°C, best fit straight line		0.05		°/s/K

Output Noise	$n_{G,nD}$	@10 Hz		0.007		°/s/√Hz
	$n_{G,rms}$	Filter setting 74.6Hz, ODR 200 Hz		0.07		°/s rms
Bias stability	BS_G			10		°/h
Output Data Rate (set of x,y,z rate)	ODR_G		25		3200	Hz
Output Data Rate (set of x,y,z rate)	ODR_{OIS}	Fixed setting		6400		Hz
Output Data rate accuracy (set of x,y,z rate)	$AODR_G$	Over whole operating temperature range		±1		%
Cross Axis Sensitivity	$X_{G,S}$	Sensitivity to stimuli in non-sense-direction			2	%

Table 4: Electrical characteristics temperature sensor

OPERATING CONDITIONS AND OUTPUT SIGNAL OF TEMPERATURE SENSOR						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Temperature Sensor Measurement Range	T_S		-40		85	°C
Temperature Sensor Slope	dT_S			0.002		K/LSB
Temperature Sensor Offset	OT_S			±2		K
Output Data Rate	ODR_T	gyro in fast start-up		0.8		Hz
		Gyro active		100		Hz
Resolution	n_T	gyro in fast start-up		8		bit
		Gyro active		16		Bit

2.3 Absolute maximum ratings

Table 5: Absolute maximum ratings

Parameter	Condition	Min	Max	Units
Voltage at Supply Pin	V_{DD} Pin	-0.3	4.25	V
	V_{DDIO} Pin	-0.3	4.25	V
Voltage at any Logic Pin	Non-Supply Pin	-0.3	V_{DDIO}+0.3	V
Passive Storage Temp. Range	≤65% rel. H.	-50	+150	°C
None-volatile memory (NVM) Data Retention	T = 85°C, after 15 cycles	10		y
Mechanical Shock	Duration 200 µs, half sine		10,000	g
	Duration 1.0 ms, half sine		2,000	g
	Free fall onto hard surfaces		1.8	m
ESD	HBM, at any Pin		2	kV
	CDM		500	V
	MM		200	V

Note: Stress above these limits may cause damage to the device. Exceeding the specified electrical limits may affect the device reliability or cause malfunction.

3. Functional Description

3.1 Block diagram

The figure below depicts the dataflow in BMG250:

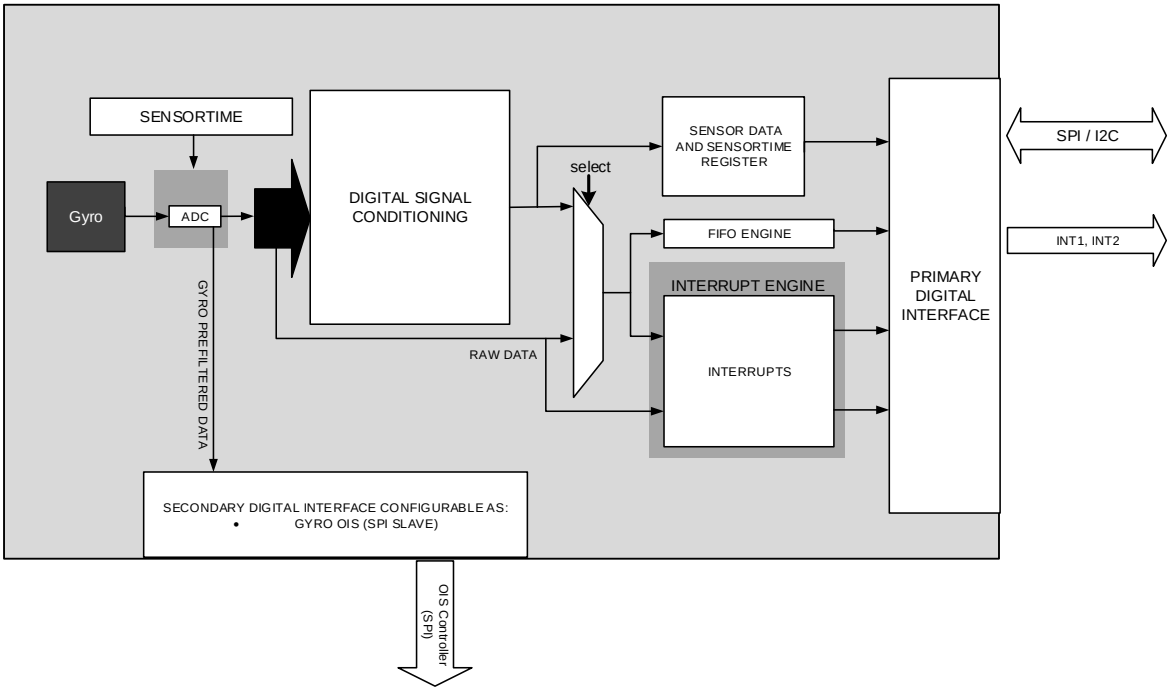


Figure 1: Block diagram of data flow

The pre-filtered input data may be already temperature compensated or other low level correction operations may be applied to them.
The data from the sensor are always sampled with a data rate of 6400 Hz. The data are low pass filtered at an output data rate as configured in the Register (0x42) GYR_CONF. In addition further down sampling for the interrupt engines and the FIFO is possible and configured in the Register (0x45) FIFO_DOWNS. This down sampling discards data frames.
The sensor time is synchronized with the update of the data register.

3.2 Power modes

By default the BMG250 is in suspend mode after powering up the device. From there, the device will start-up to normal mode within 50ms typically. Alternatively, the device may be also held in Fast Start-up mode. The device is powering up from Fast Start-up mode in less than 10ms.

Three power modes are supported:

Gyroscope

- **Normal mode:** full chip operation
- **Suspend mode**: No sampling takes place, all data is retained, and delays between subsequent I^2C operations are allowed. FIFO data readout is not supported in suspend mode.
- **Fast start-up mode:** start-up delay time to normal mode ≤10 ms. FIFO data readout is supported in fast start-up mode, although the data will only be generated during normal mode. This means data generated in normal mode can be read after the BMG250 has been switched to fast start-up mode. After the end of valid data is reached only values of 0x8000 can be read, which should be interpreted as “FIFO empty”. If the measured rate would be 0x8000 in reality, a 0x8001 is generated.

Table 6: Power modes of BMG250

full operation mode	Normal mode
Sleep modes	Fast Start-up mode
	Suspend mode

Suspend and fast start-up modes are *sleep modes*. Switching between normal and fast start-up mode will stop sampling of data. No valid data can be sampled in fast start-up mode. However, previously collected data in normal mode can still be read. The system can be switched from fast start-up mode to normal mode within 10ms to again sample data.

3.2.1 Suspend mode

In suspend mode, the MEMS sensor is powered off but the digital circuitry is still active.

Note:
When the sensor is in suspend or fast start-up mode, burst writes are not supported, normal writes need wait times after the write command is issued (~400 µs), and burst reads are not supported on Register (0x24) FIFO_DATA.

3.2.2 Fast start-up mode

In **fast start-up mode** the sensing analog part is powered down, while the drive and the digital part remains largely operational. No data acquisition is performed. The latest rate data and the content of all configuration registers are kept. The fast start-up mode allows a fast transition (≤10 ms) into normal mode while keeping power consumption significantly lower than in normal mode.

3.2.3 Transitions between power modes

With regard to the below diagram, transitions are allowed between any power mode.

Table 7: Typical total current consumption in µA according to the gyroscope's modes

		Current consumption in µA
Gyroscope Mode	**Suspend**	3
	Fast Start-up	500
	Normal	850

The power mode setting can be configured independently from the output data rate set. The main difference between normal and Fast Start-up mode is the power consumption which is in the Fast Start-up mode determined by the drive circuitry and the IO communication.

3.2.4 PMU (Power Management Unit)

The integrated PMU (Power Management Unit) allows advanced power management features by combining power management features of the sensor and externally available wake-up devices. See chapter 3.6.2 PMU Trigger (Gyro).

3.2.4.1 Automatic gyroscope power mode changes

To further lower the power consumption, the gyroscope may be configured to be temporarily put into sleep mode, which is in BMG250 configurable as suspend or fast-start-up mode. To configure this feature Register (0x6C) PMU_TRIGGER is used.

3.3 Sensor Timing and Data synchronization

3.3.1 Sensor Time

The Register (0x18-0x1A) SENSORTIME is a free running counter, which increments with a resolution of 39 µs. All sensor events e.g. updates of data registers are synchronous to this register as defined in the table below. With every update of the data register or the FIFO, a bit *m* in the Register (0x18-0x1A) SENSORTIME toggles where *m* depends on the output data rate for the data register and the output data rate and the FIFO down sampling rate for the FIFO. The table below shows which bit toggles for which update rate of data register and FIFO. The time stamps in Register (0x18-0x1A) SENSORTIME are available independent of the power mode the device is in.

Table 11: Sensor time

Bit *m* in sensor_time	Resolution [ms]	Update rate [Hz]
0	0.039	25641
1	0.078	12820
2	0.156	6400
3	0.3125	3200
4	0.625	1600
5	1.25	800
6	2.5	400
7	5	200
8	10	100
9	20	50
10	40	25
11	80	12.5
12	160	6.25
13	320	3.125
14	640	1.56
15	1280	0.78
16	2560	0.39
17	5120	0.20
18	10240	0.10
19	20480	0.049
20	40960	0.024
21	81920	0.012
22	163840	0.0061
23	327680	0.0031

3.4 Data Processing

The digital filter can be configured through the parameters: *gyr_bwp* and *gyr_odr*. There is no undersampling parameter for the gyroscope.

Note:
Illegal settings in configuration registers will result in an error code in the Register (0x02) ERR_REG. The content of the data register is undefined, and if the FIFO is used, it may contain no value.

3.4.1 Data Processing

The gyroscope data can only be processed in normal power mode.
There are three data processing modes defined by gyr_bwp. Normal mode, OSR2, OSR4. For details see chapter 3.4.1.1.

3.4.1.1 Gyroscope data processing for normal power mode

When the filter mode is set to normal (gyr_bwp=0b010), the gyroscope data is sampled at equidistant points in the time, defined by the gyroscope output data rate parameter (gyr_odr). The output data rate can be configured in one of eight different valid ODR configurations going from 25Hz up to 3200Hz.

Note: Lower ODR values than 25Hz are not allowed. If they are used they result in an error code in Register (0x02) ERR_REG.

The filter bandwidth as configured by gyr-odr shows a 3db cutoff frequency shown in the following table:

Gyroscope ODR [Hz]	**25**	**50**	**100**	**200**	**400**	**800**	**1600**	**3200**
3dB Cutoff frequency [Hz]	10.7	20.8	39.9	74.6	136.6	254.6	523.9	890

When the filter mode is set to **OSR2** (gyr_bwp=0b001), both stages of the digital filter are used and the data is oversampled with an oversampling rate of 2. That means that for a certain filter configuration, the ODR has to be 2 times higher than in the normal filter mode. Conversely, for a certain filter configuration, the filter bandwidth will be the approximately half of the bandwidth achieved for the same ODR in the normal filter mode. For example, for ODR=50Hz we will have a 3dB cutoff frequency of 10.7Hz.

When the filter mode is set to **OSR4** (gyr_bwp=0b000), both stages of the digital filter are used and the data is oversampled with an oversampling rate of 4. That means that for a certain filter configuration, the ODR has to be 4 times higher than in the normal filter mode. Conversely, for a certain filter configuration, the filter bandwidth will be approximately 4 times smaller than the bandwidth achieved for the same ODR in the normal filter mode. For example, for ODR=100Hz we will have a 3dB cutoff frequency of 10.7Hz.
There is no undersampling mode for the gyroscope data processing.

3.5 FIFO

A FIFO is integrated in BMG250 to support low power applications and prevent data loss in non-real-time systems. The FIFO has a size of 1024 bytes. The FIFO architecture supports to dynamically allocate FIFO space. For typical applications, this is sufficient for approx. 1.4s of data capture (ODR=100Hz). If a lower ODR is used, the FIFO size will be sufficient for capturing data longer, increasing ODR will reduce available capturing time. The FIFO features a FIFO full and watermark interrupt. Details can be found in chapter 3.6.3.

A schematic of the data path when the FIFO is used is shown in the figure below.

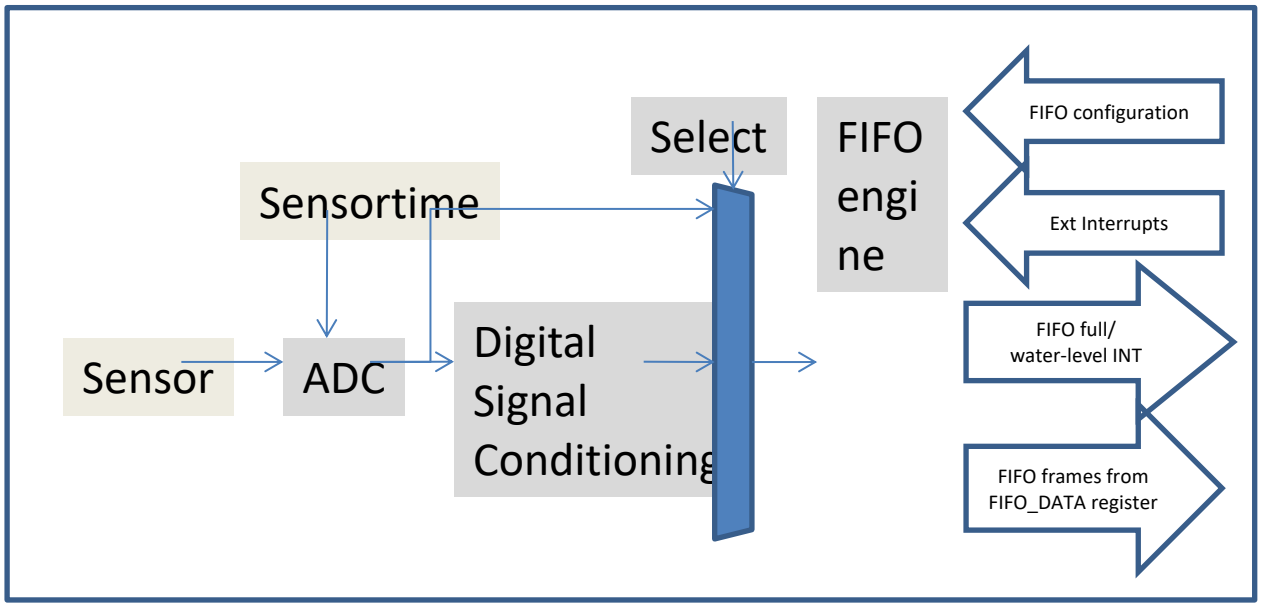


Figure 3: Block diagram of FIFO data path

3.5.1 FIFO Frames

When using the FIFO, the stored data can be read out by performing a burst read on the register (0x24) FIFO_DATA. The data is stored in units called frames.

3.5.1.1 Frame rates

The frame rate for the FIFO is defined by the maximum output data rate of the sensor via the Register (0x46-0x47) FIFO_CONFIG. If pre-filtered data are selected in Register (0x45) FIFO_DOWNS, a data rate of 6400 Hz is used.

The frame rate can be reduced further via downsampling (Register (0x45) FIFO_DOWNS). This can be done independently for each sensor. Downsampling just drops sensor data; no data processing or filtering is performed.

3.5.1.2 Frame format

When using the FIFO, the stored data can be read out by performing a burst read on the register (0x24) FIFO_DATA. The data will be stored in frames. The frame format is configurable.

The FIFO can be configured to store data in either header mode or in headerless mode (see figure below). The headerless mode is usually used when the structure of data does not change during data acquisition. In this case, the number of storable frames can be maximized. In contrast, the header mode is intended for situations where flexibility in the data structure is required, e.g. when the sensor runs at different ODRs or when switching the sensor on or off during operation.

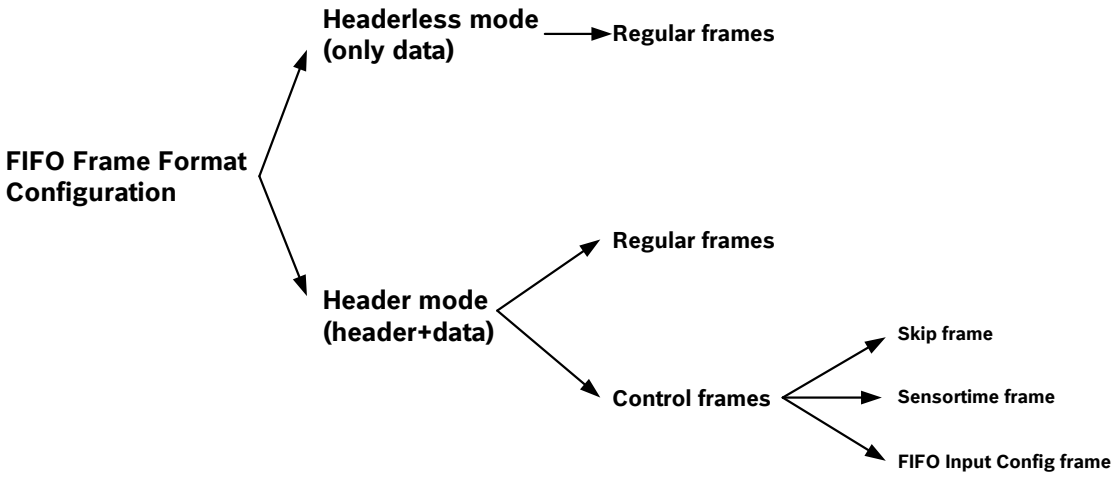


Figure 4: FIFO frame configurations

In **headerless mode** no header byte is used and the frames consist only of data bytes. The data bytes will always be sensor data. This mode has the advantage of an easy frame format and an optimized usage of the 1024 bytes of FIFO storage. It can be selected by disabling fifo_header in Register (0x46-0x47) FIFO_CONFIG. In case of overreading the FIFO, non-valid frames always contain the fixed expression (magic number) 0x80 in the data frame.

In **header mode** every frame consists of a header byte followed by one or more data bytes. The header defines the frame type and contains parameters for the frame. The data bytes may be sensor data or control data. Header mode supports different ODRs for the gyroscope data and external interrupt flags. It is activated by enabling fifo_header in Register (0x46-0x47) FIFO_CONFIG.

3.5.1.3 Header byte format

The header format is shown below:

Bit	**7**	**6**	**5**	**4**
Content	fh_mode		fh_parm<3:2>	

Bit	**3**	**2**	**1**	**0**
Read/Write	fh_parm<1:0>		fh_ext	

The *fh_mode, fh_opt* and *fh_ext* fields are defined as

fh_mode<1:0>	Definition	fh_parm <3:0>	fh_ext<1:0>
0b10	Regular	Frame content	Tag of INT2 and INT1
0b01	Control	Control Opcode	
0b00	Reserved	Na	
0b11	Reserved	Na	

f_parm=0b0000 is invalid for regular mode, a header of 0x80 indicates an uninitialized frame.

3.5.1.4 Data bytes Format

When the FIFO is set to “headerless mode“, only sensor data will be saved into the FIFO (in the same order as in the data register). External interrupt tags are not supported in headerless mode.

When the FIFO is set to “header mode“, the data byte format is different depending on the type of frame. There are two basic frame types, control frames and regular data frames. Each different type of control frame has its own data byte format. It can contain skipped frames, sensortime data or FIFO configuration information as explained in the following chapters. If the frame type is a regular frame (sensor data), the data byte section of the frame depend on how the data is being transmitted in this frame (as specified in the header byte section).

The **data byte** part for regular data frames is identical to the format defined for the Register (0x12-0x17) DATA.

Control frame (fh_mode=0b01):

Control frames, which are only available in header mode, are used for special or exceptional information. All control frames contribute to the *fifo_byte _counter* in Register (0x22-0x23) FIFO_LENGTH. In detail, there are three types of control frame, which can be distinguished by the *fh_parm* field:

Skip frame (fh_parm=0b000):
In case of a FIFO overflow, a skip frame is prepended to the FIFO content when the next readout is performed. A skip frame indicates the number of skipped frames since the last readout.
In the header byte of a skip frame, fh_mode equals 0b01 (since it is a control frame) and the fh_param equals 0b000 (indicating skip frame). The data byte part of a skip frame consists of one byte and contains the number of skipped frames. When more than 0xFF frames have been skipped, 0xFF is returned.

Sensortime frame (fh_parm=0b001):
If the sensortime frame functionality is activated (see description of Register (0x46-0x47) FIFO_CONFIG) and the FIFO is overread, the last data frame is followed by a sensortime frame. This frame contains the BMG250 timestamp content corresponding to the time at which the last data frame was read.
In the header byte of a sensortime frame, fh_mode = 0b01 (since is a control frame) and fh_param = 0b001 (indicating sensortime frame). The data byte part of a sensortime frame

consists of 3 bytes and contains the 24-bit sensortime. A sensortime frame does not consume memory in the FIFO.

FIFO_input_config frame (fh_parm=0b010):
Whenever the configuration of the FIFO input data sources changes, a FIFO input config frame is inserted into the FIFO in front of the data to which the configuration change is applied.
In the header byte of a config frame, fh_mode = 0b01 (since it is a control frame) and fh_param = 0b010 (indicating FIFO_input_config frame). The data byte part of a FIFO_Input_Config Frame consists of one byte and contains data corresponding to the following table:

Bit	7	6	5	4
Content	reserved			

Bit	3	2	1	0
Read/Write	gyr_range_ch	gyr_conf_ch	reserved	

gyr_range_ch: A change in Register (0x43) GYR_RANGE becomes active.
gyr_conf_ch: A change in Register (0x42) GYR_CONF or gyr_fifo_filt_data or gyr_fifo_downsampling in Register (0x45) FIFO_DOWNS becomes active.

3.5.2 FIFO conditions and details

3.5.2.1 Overflows

In the case of overflows the FIFO will overwrite the oldest data. A skip frame will be prepended at the next FIFO readout if the available FIFO space falls below the maximum size frame.

3.5.2.2 Overreads

If more data bytes are read from the FIFO than valid data bytes are available, ‘0x80’ is returned. Since a header ‘0x80’ indicates an invalid frame, the SW can recognize the end of valid data. After the invalid header the data is undefined. This is valid in both headerless and header mode. In addition, if header mode and the sensortime frame are enabled, the last data frame is followed by a sensortime frame. After this frame, a 0x80 header will be returned that indicates the end of valid data.

3.5.2.3 Partial frame reads

When a frame is only partially read through, it will be repeated within the next reading operation (including the header).

3.5.2.4 FIFO synchronization with external events

External events can be synchronized with the FIFO data by connecting the event source to one of the BMG250 interrupt pins (which needs to be configured as an input interrupt pin). External events can be generated e.g. by a camera module. Each frame contains the value of the interrupt input pin at the time of the external event.

The fh_ext<1:0> field is set when an external interrupt is triggered. External interrupt tags are configured using *int<x>_output_en* in Register (0x53) INT_OUT_CTRL.

3.5.2.5 FIFO Reset

A reset of the BMG250 is triggered by writing the opcode 0xB0 “fifo_flush“ to the Register (0x7E) CMD. This will clear all data in the FIFO while keeping the FIFO settings unchanged.
Automatic resets are only done in two exceptional cases where the data would not be usable without a reset:

- a sensor is enabled or disabled in headerless mode, or
- a transition between headerless and header mode occurred.

3.5.2.6 Error Handling

In case of a configuration error in Register (0x46-0x47) FIFO_CONFIG, no data will be written into the FIFO and the error is reported in Register (0x02) ERR_REG.

3.6 Interrupt Controller

There are 2 interrupt output pins, to which 3 different interrupt signals can be mapped independently via user programmable parameters.

Available interrupts in normal mode are:

- **Data ready ("new-data")** for synchronizing sensor data read-out with the MCU / host controller
- **FIFO full / FIFO watermark** allows FIFO fill level and overflow handling.

All Interrupts are available only in normal (low-noise) mode, but not in suspend mode.

Input Interrupt Pins: For special applications (e.g. PMU Trigger, FIFO Tag) interrupt pins can be configured as input pins. For all other cases (standard interrupts), the pin must be configured as an output.

Note: The direction of the interrupt pins is controlled with *int<x>_output_en* and *int_x_input_en* in Register (0x53) INT_OUT_CTRL and Register (0x54) INT_IN_CTRL. If both are enabled, the input (e.g. marking fifo) is driven by the interrupt output.

3.6.1 Data Ready Detection

This interrupt is enabled whenever a new data sample is complete. This allows a low latency data readout.
The data update detection monitors the *data_update* signals for all axes. It generates an interrupt as soon as the values for all axes which are required for the configured output data rates have been updated.
The interrupt is cleared automatically when the update for the next sample starts or the data is read out from the data register.

3.6.2 PMU Trigger (Gyro)

Whenever a PMU (power management unit) trigger (either wakeup or sleep) is issued, *wakeup_int* in Register (0x6C) PMU_TRIGGER configures if an interrupt is send to the application processor. If the AP wants to trigger sleeps itself for the gyro, the *gyr_wakeup_trigger* is configured accordingly and no wakeup triggers are issued.

3.6.3 FIFO Interrupts

The FIFO supports two interrupts, a FIFO full interrupt and a watermark interrupt. The FIFO full interrupt is issued when the FIFO is full and the next full data sample would cause a FIFO overflow, which may lead to samples being deleted. Technically, that means that a FIFO full interrupt is issued, whenever less space than two maximum size frames is left in the FIFO. The FIFO watermark interrupt is fired, when the FIFO fill level in *fifo_byte_counter* in Register (0x22-0x23) FIFO_LENGTH is above a pre-configured watermark, defined in *fifo_watermark* in Register (0x46-0x47) FIFO_CONFIG.

Note: The unit of *fifo_watermark* is 4 bytes whereas the unit of *fifo_byte_counter* is single bytes.

3.7 Device self test

This feature permits to check the sensor functionality via a built-in self-test (BIST).
The BIST can be triggered during normal operation mode. It checks the sensors drive amplitude, its frequency and the stability of the drive control loop. Hence, disturbances of the movement by particles, mechanical damage or pressure loss can be detected.
The self-test for the gyroscope will be started by writing a '1' to *gyr_self_test_enable* in Register (0x6D) SELF_TEST. The result will be in *gyr_self_test_ok* in Register (0x1B) STATUS.

In addition, any particles or damages can be easily identified in a „Manual Performance Check". Due to the outstanding offset and noise performance the measured values at zero-rate fit the specified performance.

3.8 Offset Compensation

BMG250 offers fast and manual compensation as well as inline calibration.
Fast offset compensation is performed with pre-filtered data, and the offset is then applied to both, pre-filtered and filtered data. If necessary the result of this computation is saturated to prevent any overflow errors (the smallest or biggest possible value is set, depending on the sign).
The public offset compensation Register (0x74-0x77) OFFSET are images of the corresponding registers in the NVM. With each image update the contents of the NVM registers are written to the public registers. The public registers can be overwritten by the user at any time. Offset compensation needs to be enabled through *gyr_off_en* (Register 0x77).

3.8.1 Fast offset compensation

Fast offset compensation (FOC) is a one-shot process that compensates offset errors by setting the offset compensation registers to the negated offset error. This is best suited for “end-of-line trimming” with the customers device positioned in a well-defined orientation.
The Gyroscope target value is always 0 dps at rest.

FOC is triggered by issuing a *start_foc* command to Register (0x7E) CMD. Once triggered, the status of the fast correction process is reflected in the status bit *foc_rdy* in
Register (0x1B) STATUS. *foc_rdy* is ‘0’ while the measurement is in progress. Preset filter settings apply. This will take a maximum time of 250 ms.
The negated measured values are written to Register (0x74-0x77) OFFSET automatically (overwriting previous offset register values), cancelling out offset errors.
Fast compensation can only be used in normal mode.
The fast offset compensation does not automatically clear the data ready bit in Register (0x1B) STATUS. It is recommended to read the Register (0x12-0x17) DATA after FOC completes, to remove a stall data ready bit from before the FOC. In this way the data ready bit can be made functional again to indicate that the next sample is available for reading, while using data from the FOC mechanism.

3.8.2 Manual offset compensation

The contents of the public compensation Register (0x74-0x77) OFFSET may be set manually via the digital interface. After modifying the Register (0x74-0x77) OFFSET the next data sample is not valid.
Writing to the offset compensation registers is not allowed while the fast compensation procedure is running.

3.8.3 Inline calibration

For certain applications, it is often desirable to calibrate the offset once and to store the compensation values permanently. This can be achieved by using fast or manual offset compensation to determine the proper compensation values and then storing these values permanently in the NVM.

Each time the device is reset, the compensation values are loaded from the non-volatile memory into the image registers and used for offset compensation.

3.9 Non-Volatile Memory

The memory of the BMG250 consists of volatile and non-volatile registers. Part of it can be both read and written by the user. Access to non-volatile memory is only possible through (volatile) image registers.

A maximum number of write cycles to non-volatile memory of equal or less than 14 is supported.

The Register (0x70) NV_CONF and Register (0x74-0x77) OFFSET have NVM backups which are accessible by the user.
The content of the NVM is loaded to the image registers after a reset (either POR or softreset). As long as the image update is in progress, bit *nvm_rdy* in
Register (0x1B) STATUS is ´0´, otherwise it is ´1´.

The image registers can be read and written like any other register.

Writing to the NVM is a four-step procedure:
Write “0x11” into CMD (0x7E) register to make sensor enter NORMAL power state.
Write the new contents to the image registers.
Write ´1´ to bit *nvm_prog_en in the* Register (0x6A) CONF register in order to unlock the NVM.
Write prog_nvm (0xA0) to the Register (0x7E) CMD to trigger the write process.

Writing to the NVM always renews the entire NVM contents. It is possible to check the write status by reading bit *nvm_rdy*. While *nvm_rdy* = ´0´, the write process is still in progress; if *nvm_rdy* = ´1´, then writing is completed. As long as the write process is ongoing, no change of power mode and image registers is allowed.

After *nvm_rdy* turns to be ´1´, user can optionally write “0x10” into CMD (0x7E) register to switch power status back into suspend mode, if needed.

3.10 Register Map

This chapter contains register definitions. REG[x]<y> denotes bit y in byte x in register REG. Val(Name) is the value contained in the register interpreted as non-negative binary number. When writing to reserved bits, '0' should be written when not stated different.

read/write	read only	write only	reserved

Register Address	Register Name	Default Value	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x007D	-	-	reserved							
0x0078	-	-	reserved							
0x0077	OFFSET_6	0x00	gyr_off_en	reserved	off_gyr_z_9_8		off_gyr_y_9_8		off_gyr_x_9_8	
0x0076	OFFSET_5	0x00	off_gyr_z_7_0							
0x0075	OFFSET_4	0x00	off_gyr_y_7_0							
0x0074	OFFSET_3	0x00	off_gyr_x_7_0							
0x0073	-	-	reserved							
0x0071	-	-	reserved							
0x0070	NV_CONF	0x00	reserved					i2c_wdt_en	i2c_wdt_sel	spi_en
0x006F	-	-	reserved							
0x006E	-	-	reserved							
0x006D	SELF_TEST	0x00	reserved			gyr_self_test_start	reserved			
0x006C	PMU_TRIGGER	0x10	reserved		gyr_sleep_state	reserved	gyr_wakeup_trigg	reserved	gyr_sleep_trigger	
0x006B	IF_CONF	0x00	reserved		reserved	if_mode	reserved			spi3
0x006A	CONF	0x00	reserved						nvm_prog_en	reserved
0x0069	-	-	reserved							
0x0057	-	-	reserved							
0x0056	INT_MAP_1	0x00	int1_drdy	int1_fwm	int1_ffull	reserved	int2_drdy	int2_fwm	int2_ffull	reserved
0x0055	-	-	reserved							
0x0054	INT_LATCH	0x00	reserved		int2_input_en	int1_input_en	reserved			
0x0053	INT_OUT_CTRL	0x00	int2_output_en	int2_od	int2_lvl	int2_edge_ctrl	int1_output_en	int1_od	int1_lvl	int1_edge_ctrl
0x0052	-	-	reserved							
0x0051	INT_EN_1	0x00	reserved	int_fwm_en	int_ffull_en	int_drdy_en	reserved			
0x0050	-	-	reserved							
0x0048	-	-	reserved							
0x0047	FIFO_CONFIG_1	0x10	fifo_gyr_en	reserved		fifo_header_en	fifo_tag_int1_e	fifo_tag_int2	fifo_time_en	fifo_stop_on_full
0x0046	FIFO_CONFIG_0	0x80	fifo_water_mark							
0x0045	FIFO_DOWNS	0x88	reserved				gyr_fifo_filt_dat	gyr_fifo_downs		
0x0044	-	-	reserved							
0x0043	GYR_RANGE	0x00	reserved					gyr_range		
0x0042	GYR_CONF	0x28	reserved		gyr_bwp		gyr_odr			
0x0041	-	-	reserved							
0x0025	-	-	reserved							
0x0024	FIFO_DATA	0x00	fifo_data							
0x0023	FIFO_LENGTH_1	0x00	reserved					fifo_byte_counter_10_8		
0x0022	FIFO_LENGTH_0	0x00	fifo_byte_counter_7_0							
0x0021	TEMPERATURE_1	0x80	temperature_15_8							
0x0020	TEMPERATURE_0	0x00	temperature_7_0							
0x001F	-	-	reserved							
0x001E	-	-	reserved							
0x001D	INT_STATUS_1	0x00	reserved	fwm_int	ffull_int	drdy_int	reserved			
0x001C	-	-	reserved							
0x001B	STATUS	0x01	reserved	drdy_gyr	reserved	nvm_rdy	foc_rdy	reserved	gyr_self_test_ok	reserved
0x001A	SENSORTIME_2	0x00	sensor_time_23_16							
0x0019	SENSORTIME_1	0x00	sensor_time_15_8							
0x0018	SENSORTIME_0	0x00	sensor_time_7_0							
0x0017	DATA_19	0x00	gyr_z_15_8							
0x0016	DATA_18	0x00	gyr_z_7_0							
0x0015	DATA_17	0x00	gyr_y_15_8							
0x0014	DATA_16	0x00	gyr_y_7_0							
0x0013	DATA_15	0x00	gyr_x_15_8							
0x0012	DATA_14	0x00	gyr_x_7_0							
0x0011	-	-	reserved							
0x0004	-	-	reserved							
0x0003	PMU_STATUS	0x00	reserved		tmp_pmu_status		gyr_pmu_status		reserved	
0x0002	ERR_REG	0x00	reserved	drop_cmd_e	reserved	err_code				fatal_err
0x0001	-	-	reserved							
0x0000	CHIP_ID	0xD5	chip_id							

3.10.1 Register (0x00) CHIPID

ADDRESS 0x00
RESET 0xD5
MODE R
DESCRIPTION The register contains the chip identification code.
DEFINITION

Name		**Register (0x00) CHIPID**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	1	1	0	1
Content	chip_id<7:4>			
Bit	**3**	**2**	**1**	**0**
Read/Write	R	R	R	R
Reset Value	0	1	0	1
Content	chip_id<3:0>			

3.10.2 Register (0x02) ERR_REG

ADDRESS 0x02
RESET 0b00000000
MODE RW
DESCRIPTION Reports sensor error flags. Flags are reset when read.

DEFINITION

Bit	Acronym	Definition
7	Reserved	
6	drop_cmd_err	Dropped command to Register
5	Reserved	
4:1	error_code	0000: no error 0001: reserved 0010: gyr conf error 0010-1111: reserved The first reported error will be shown in the error code.
0	fatal_err	Chip not operable. The only way to clear the flag is a POR or soft-reset.

The register is meant for debug purposes, not for regular verification if an operation completed successfully.

Error flags (bits 4:1) store error event until they are reset by reading the register.

3.10.3 Register (0x03) PMU_STATUS

ADDRESS 0x03
RESET 0b0000-0000
MODE R
DESCRIPTION Shows the current power mode of the sensor.
DEFINITION

Name		**Register (0x03) PMU_STATUS**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	reserved			
Bit	**3**	**2**	**1**	**0**
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	gyr_pmu_status		reserved	

gyr_pmu_status	**Gyro Mode**
0b00	Suspend
0b01	Normal
0b10	Reserved
0b11	Fast Start-Up

The register reflects the current power modes of all sensor configured as soon as they are effective. If a sensor is enabled, the new sensor mode is reported as soon as the MEMS is up and before digital filters have settled. The settling time depends on filter settings. The power modes may be changed through the Register (0x7E) CMD. In addition, for the gyroscope through register events may be defined, which change the gyro power mode.

In suspend mode the FIFO is not accessible. For read outs of the FIFO the sensor has to be set to normal mode, after read-out the sensor can be set back suspend or fast start-up mode.

3.10.4 Register (0x12-0x17) DATA

ADDRESS 0x12 (6 bytes)
RESET (BYTEWISE) 0b0000-0000
MODE R
DESCRIPTION Register for gyroscope data. DATA[0-5] are treated as atomic update unit with respect to an I²C/SPI operation. A read operation on the Register (0x12-0x17) DATA resets the appropriate *_drdy bits in
Register (0x1B) STATUS. E.g. when only [0] is read, only *drdy_gyr* is reset.
DEFINITION
DATA[0-5] contains the latest data for the gyroscope GYR_[X-Z].
If the secondary interface (OIS interface, working in SPI protocol) is connected, the OIS data are accessible through Register (0x012-0x17) for OIS_DATA_[X/Y/Z]_[0/1].

DATA[X]	Acronym
X=0	GYR_X<7:0> (LSB)
X=1	GYR_X<15:8> (MSB)
X=2	GYR_Y<7:0> (LSB)
X=3	GYR_Y<15:8> (MSB)
X=4	GYR_Z<7:0> (LSB)
X=5	GYR_Z<15:8> (MSB)

OIS_DATA[AXIS]_[MSB]	Acronym
AXIS = X, MSB = 0	OIS_DATA_X<7:0> (LSB)
AXIS = X, MSB = 1	OIS_DATA _X<15:8> (MSB)
AXIS = Y, MSB = 0	OIS_DATA _Y<7:0> (LSB)
AXIS = Y, MSB = 1	OIS_DATA _Y<15:8> (MSB)
AXIS = Z, MSB = 0	OIS_DATA _Z<7:0> (LSB)
AXIS = Z, MSB = 1	OIS_DATA _Z<15:8> (MSB)

3.10.5 Register (0x18-0x1A) SENSORTIME

ADDRESS 0x18 (3 byte)
RESET 0x00_0000
MODE R
DESCRIPTION Sensortime is a 24 bit counter available in suspend, low power, and normal mode. The value of the register is shadowed when it is read in a burst read with the data register at the beginning of the operation and the shadowed value is returned. When the FIFO is read the register is shadowed whenever a new frame is read.
DEFINITION The sensortime increments with 39 µs. The accuracy of the counter is the same as for the output data rate as described in section 2.2. The sensortime is unique for approx. 10 min and 54 seconds. I.e. the register value starts at 0x000000 and wraps after 0xFFFFFF has been reached.

Name		**Register (0x18-0x1A) SENSORTIME [0]**		
Bit	7	6	5	4
Read/Write	W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	sensor_time<7:4>			

Bit	**3**	**2**	**1**	**0**
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	sensor_time<3:0>			

Name		**Register (0x18-0x1A) SENSORTIME [1]**		
Bit	7	6	5	4
Read/Write	W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	sensor_time<15:11>			

Bit	**3**	**2**	**1**	**0**
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	sensor_time<10:8>			

Name		**Register (0x18-0x1A) SENSORTIME [2]**		
Bit	7	6	5	4
Read/Write	W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	sensor_time<23:19>			

Bit	**3**	**2**	**1**	**0**
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	sensor_time<19:16>			

3.10.6 Register (0x1B) STATUS

ADDRESS 0x1B
RESET 0b00000000
MODE RW
DESCRIPTION Reports sensor status flags.
DEFINITION

Bit	Acronym	Definition
7	reserved	
6	drdy_gyr	Data ready (DRDY) for gyroscope in register
5	reserved	
4	nvm_rdy	NVM controller status
3	foc_rdy	FOC completed
2	reserved	
1	gyr_self_test_ok	'0' when gyroscope self-test is running or failed. '1' when gyroscope self-test completed successfully.
0	por_detected	'0' after read, '1' after software reset or power on

drdy_*: gets reset when one byte of the register for sensor * is read.

nvm_rdy: status of NVM controller: ´0´ → NVM write operation is in progress; ´1´ → NVM is ready to accept a new write trigger

foc_rdy: Fast offset compensation completed

3.10.7 Register (0x1D) INT_STATUS_1

ADDRESS 0x1D (1 byte)
RESET
MODE RW
DESCRIPTION The register contains interrupt status flags.

DEFINITION
Each flag is associated with a specific interrupt function. It is set when the associated interrupt triggers. The interrupt function associated with a specific status flag must be enabled.

Register (0x1D) INT_STATUS_1		definition
6	fwm_int	Fifo watermark
5	ffull_int	Fifo full
4	drdy_int	Data ready

'0' interrupt inactive, '1' interrupt active.

3.10.8 Register (0x20-0x21) TEMPERATURE

ADDRESS 0x20 (2 byte)
RESET 0x8000 (-128°C)
MODE R
DESCRIPTION Contains the temperature of the sensor
DEFINITION
The output word of the 16-bit temperature sensor is only valid if the gyroscope is in normal mode, i.e. *gyr_pmu_status*=0b01. The resolution is typically $1/2^9$ K/LSB.

Value	Temperature
0x7FFF	87 – $1/2^9$ °C
…	…
0x0000	23 °C
…	…
0x8001	-41 + $1/2^9$ °C
0x8000	Invalid

If the gyroscope is in normal mode (see Register (0x03) PMU_STATUS), the temperature is updated every 10 ms (+-12%).
Otherwise, when the gyroscope is in suspend mode and TMP power state is in normal mode, the temperature is updated every 1.28s aligned with bit 15 of the Register (0x20-0x21) TEMPERATURE.
Another configuration is that, when the gyroscope is in fast-power up mode, but TMP power state is set to suspend mode, the temperature measurement will also be executed every 1.28s and Register (0x20-0x21) TEMPERATURE will be updated accordingly.
Comparatively, when both the gyroscope and TMP power states are set to suspend mode, the temperature measurement will be disabled and will not be executed.

3.10.9 Register (0x22-0x23) FIFO_LENGTH

ADDRESS 0x22 (2 byte)
RESET 0x0000
MODE R
DESCRIPTION FIFO data readout register.
DEFINITION
The register contains FIFO status flags.

Name		**Register (0x22-0x23) FIFO_LENGTH [0]**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	fifo_byte_counter<7:4>			

Bit	**3**	**2**	**1**	**0**
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	fifo_byte_counter<3:0>			

Name		**Register (0x22-0x23) FIFO_LENGTH [1]**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	Reserved			

Bit	**3**	**2**	**1**	**0**
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	reserved	fifo_byte_counter<10:8>		

fifo_byte_counter: Current fill level of FIFO buffer. This includes the skip frame for a full FIFO. The FIFO counter also includes the number of skipped frames. E.g. after the FIFO is full, the counter may also reach values larger than what can actually be stored in the FIFO. An empty FIFO corresponds to 0x000. The byte counter may be reset by reading out all frames from the FIFO buffer or when the FIFO is reset through the Register (0x7E) CMD. The byte counter is updated, when a complete frame is read or written.

3.10.10 Register (0x24) FIFO_DATA

ADDRESS 0x24
RESET 0x00
MODE R
DESCRIPTION FIFO data readout register.
DEFINITION

The FIFO data are organized in frames as described in chapter 3.5.1. The new data flag is preserved. Read burst access must be used, the address will not increment when the read burst reads at the address of FIFO_DATA. When a frame is only partially read out it will be retransmitted (including the header in header mode) at the next readout. New data will only be present after the complete frame has been read.

Name		**Register (0x24) FIFO_DATA**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	fifo_data<7:4>			
Bit	**3**	**2**	**1**	**0**
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	fifo_data<3:0>			

fifo_data<7:0>: FIFO data readout; data format depends on the setting of Register (0x46-0x47) FIFO_CONFIG.

3.10.11 Register (0x42) GYR_CONF

ADDRESS 0x42
RESET 0b00101000
MODE RW
DESCRIPTION Sets the output data rate, the bandwidth, and the read mode of the gyroscope in the sensor. DEFINITION

Name		Register (0x42) GYR_CONF		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0
Content	reserved		gyr_bwp	
Bit	**3**	**2**	**1**	**0**
Read/Write	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0
Content	gyr_odr			

gyr_odr: defines the output data rate of the gyro in the sensor. This is independent of the power mode setting for the sensor. Settings below = ODR 25 Hz are illegal. The output data rate in Hz is given by $100/2^{8\text{-val(gyr\_odr)}}$.

gyr_odr	Output data rate in Hz
0b0000	Reserved
0b0001	Reserved
0b0010	Reserved
...	(all reserved)
0b0101	Reserved
0b0110	25
...	
0b1000	100
...	
0b1100	1600
0b1101	3200
0b111x	Reserved

gyr_bwp: the gyroscope bandwidth coefficient defines the 3 dB cutoff frequency of the low pass filter for the sensor data. For details see Section 3.4.1.

Configurations without a bandwidth number are illegal settings and will result in an error code in the Register (0x02) ERR_REG.

3.10.12 Register (0x43) GYR_RANGE

ADDRESS 0x43
RESET 0b00000000
MODE RW
DESCRIPTION Defines the BMG250 angular rate measurement range
DEFINITION
A measurement range is selected by setting the range bits as follows:

Name		**Register (0x43) GYR_RANGE**		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	Reserved			

0

Bit	**3**	**2**	**1**	**0**
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	reserved	gyr_range<2:0>		

range[2:0]	Full Scale	Resolution
‘000’	±2000°/s	16.4 LSB/°/s ⇔ 61.0 m°/s / LSB
‘001’	±1000°/s	32.8 LSB/°/s ⇔ 30.5 m°/s / LSB
‘010’	±500°/s	65.6 LSB/°/s ⇔ 15.3 m°/s / LSB
‘011’	±250°/s	131.2 LSB/°/s ⇔ 7.6 m°/s / LSB
‘100’	±125°/s	262.4 LSB/°/s ⇔ 3.8m°/s / LSB
‘101’, ´110´, ´111´	reserved	

gyr_range<2:0>: Angular Rate Range and Resolution.

reserved: write ‘0’

Changing the range of the gyroscope does not clear the data ready bit in the Register (0x1B) STATUS. It is recommended to read the Register (0x12-0x17) DATA after the range change to remove a stall data ready bit from before the range change.

3.10.13 Register (0x45) FIFO_DOWNS

ADDRESS 0x45 (1 byte)
RESET 0b0000-0000
MODE RW
DESCRIPTION Used to configure the down sampling ratios of the data for FIFO.
DEFINITION The downsampling ratio for the data are given by $2^{Val(gyr\_fifo\_downs)}$. [gyr]*_fifo_filt_data=0 (1)* selects pre-filtered (filtered) data for the FIFO, respectively.

Name		**Register (0x45) FIFO_DOWNS**		
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			
Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0
Content	gyr_fifo_filt_data	gyr_fifo_downs		

3.10.14 Register (0x46-0x47) FIFO_CONFIG

ADDRESS 0x46 (2 bytes)
RESET 0x80 (FIFO_CONFIG[0]), 0x10 (FIFO_CONFIG[1])
MODE RW
DESCRIPTION The Register (0x46-0x47) FIFO_CONFIG is a read/write register and can be used for reading or setting the current FIFO watermark level. This register can also be used for setting the different modes of operation of the FIFO, e.g. which data is going to be stored in it and which format is going to be used (header or headerless mode).
DEFINITION

Name		**Register (0x46-0x47) FIFO_CONFIG [0]**		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0
Content	fifo_water_mark <7:4>			
Bit	**3**	**2**	**1**	**0**
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	fifo_water_mark <3:0>			

fifo_water_mark <7:0>: *fifo_water_mark* defines the FIFO watermark level. An interrupt will be generated, when the number of entries in the FIFO exceeds *fifo_water_mark*. The unit of *fifo_water_mark* are 4 bytes.

Name		**Register (0x46-0x47) FIFO_CONFIG [1]**				
Bit	7	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	0
Content	fifo_gyr_en	fifo_header_en	fifo_tag_int1_en	fifo_tag_int2_en	fifo_time_en	fifo_stop_on_full

When all the sensors are disabled, the FIFO is disabled and no headers are written. The sensors can be disabled via *fifo_gyr_en* respectively.

fifo_gyr_en: '0' no gyro data are stored in FIFO, '1' gyro data are stored in FIFO (all 3 axes)
fifo_header_en: If '1' each frame contains a header as defined in section 3.5.1. If '0' the frame format will be headerless.
fifo_tag_int1_en: 1' ('0') enables (disables) FIFO tag (interrupt)
fifo_tag_int2_en: 1' ('0') enables (disables) FIFO tag (interrupt)
fifo_time_en: '1'('0') returns (does not return) a sensortime frame after the last valid frame when more data are read than valid frames are in the FIFO.
fifo_stop_on_full: stop writing samples into FIFO when FIFO is full.

3.10.15 Register (0x51) INT_EN

ADDRESS 0x51 (1 byte)
RESET
0b0000-0000
MODE RW
DESCRIPTION Controls which interrupt engines are enabled.
DEFINITION

Register (0x51) INT_EN [1]	acronym	definition
7		Reserved
6	int_fwm_en	FIFO watermark
5	int_ffull_en	FIFO full
4	int_drdy_en	Data ready

3.10.16 Register (0x53) INT_OUT_CTRL

ADDRESS 0x53
RESET 0b0000-0000
MODE RW
DESCRIPTION Contains the behavioral configuration (electrical definition of the interrupt pins.
DEFINITION

Register (0x53) INT_OUT_CTRL	Acronym	definition
7	int2_output_en	Output enable for INT2 pin, select '0'→output disabled, or '1' →output enabled
6	int2_od	select '0'→push-pull, or '1' →open drain behavior for INT2 pin. Only valid if int2_output_en=1.
5	int2_lvl	'0'→active low, or '1'→active high level for INT2 pin. If int2_output_en=1 this applies for interrupt outputs, if int2_output_en=0 this applies to trigger PMU configured in Register (0x6C) PMU_TRIGGER. For tagging a frame in FIFO through fifo_tag_int2_en in Register (0x46-0x47) FIFO_CONFIG the setting of int2_lvl is not relevant.
4	int2_edge_crtl	'1' ('0') is edge (level) triggered for INT2 pin
3	int1_output_en	Output enable for INT1 pin, select '0'→output disabled, or '1' →output enabled
2	int1_od	select '0'→push-pull, or '1' →open drain behavior for INT1 pin. Only valid if int1_output_en=1
1	int1_lvl	select '0'→active low, or'1'→active high level for INT1 pin. If int1_output_en=1 this applies for interrupt outputs, if int1_output_en=0 this applies to trigger PMU configured in Register (0x6C) PMU_TRIGGER. For tagging in FIFO through fifo_tag_int2_en in Register (0x46-0x47) FIFO_CONFIG the setting of int2_lvl is not relevant. For tagging a frame in FIFO through fifo_tag_int1_en in Register (0x46-0x47) FIFO_CONFIG the setting of int1_lvl is not relevant.
0	int1_edge_crtl	'1' ('0') is edge (level) triggered for INT1 pin

int<x>_edge_crtl is only relevant for *int<x>_output_en* ='1'

3.10.17 Register (0x54) INT_IN_CTRL

ADDRESS 0x54
RESET 0b0000-0000
MODE RW
DESCRIPTION Contains the interrupt input mode selection.
DEFINITION
Not applied to new data

Register (0x54) INT_IN_CTRL	MODE	Definition
<7:6>	n/a	Reserved
5	RW	Input enable for INT2 pin, select '0'→input disabled, or '1' →input enabled
4	RW	Input enable for INT1 pin, select '0'→input disabled, or '1' →input enabled
<3:0>	RW	Reserved

3.10.18 Register (0x56) INT_MAP

ADDRESS 0x56 (1 byte)
RESET
0b0000-0000
MODE RW
DESCRIPTION Controls which interrupt signals are mapped to the INT1 and INT2 pin.
DEFINITION
The tables show bit number of a register and meaning of the interrupt pin.

Register (0x56) INT_MAP [1]<7:4>	Interrupt mapped to pin INT1
7	Data ready
6	FIFO watermark
5	FIFO full
4	reserved

Register (0x56) INT_MAP [1]<3:0>	Interrupt mapped to pin INT2
3	Data ready
2	FIFO watermark
1	FIFO full
0	reserved

'1' means mapping is active, '0' means mapping is inactive.
When the external interrupt is mapped to an interrupt pin, all other interrupt mappings are disabled for this interrupt. When an external interrupt is mapped to an interrupt pin, no other interrupts may be enabled.

3.10.19 Register (0x6A) CONF

ADDRESS 0x6A
RESET 0b00000000
MODE RW
DESCRIPTION Configuration of the sensor
DEFINITION

Register (0x6A) CONF Bit	Acronym	Definition
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	nvm_prog_en	Enable NVM programming
0	Reserved	

nvm_prog_en: ‘1’(‘0’) enables (disables) that the NVM may be programmed

3.10.20 Register (0x6B) IF_CONF

ADDRESS 0x6B
RESET 0x00
MODE RW
DESCRIPTION Contains settings for the digital interface.
DEFINITION

Name		Register (0x6B) IF_CONF		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	Reserved		if_mode	
Bit	**3**	**2**	**1**	**0**
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	Reserved			spi3

reserved: write ‘0’
spi3: select ´0´ → 4-wire SPI, or ´1´ → 3-wire SPI mode
if_mode: 00: primary interface: autoconfig / secondary interface: off
01: Primary interface: I2C / secondary interface:OIS
10: reserved
11: reserved

3.10.21 Register (0x6C) PMU_TRIGGER

ADDRESS 0x6C
RESET 0b0001-0000
MODE RW
DESCRIPTION Used to set the trigger conditions to change the gyro power modes
DEFINITION
The *pmu_gyr_mode* in Register (0x03) PMU_STATUS is updated with each transition triggered.

Name		**Register (0x6C) PMU_TRIGGER**		
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	Reserved	wakeup_int	gyr_sleep_state	Reserved

Bit	**3**	**2**	**1**	**0**
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	gyr_wakeup_trigger<0>	Reserved	gyr_sleep_trigger	

gyr_wakeup_trigger: when both trigger conditions are enabled, both conditions must be active to trigger the transition.

gyr_wakeup_trigger	**INT1 pin**
0b0	no
0b1	yes

gyr_sleep_trigger: when more than one trigger condition is enabled, one is sufficient to trigger the transition.

gyr_sleep_trigger	**Not INT1 pin**	**INT2 pin**
0b00	no	no
0b01	no	yes
0b10	yes	no
0b11	yes	yes

If gyr_sleep_trigger and gyr_wakeup_trigger are active at the same time, the gyr_wakeup_trigger wins.

The INTx pin takes into account the edge/level triggered setting in the Register (0x53) INT_OUT_CTRL.

gyr_sleep_state: ‘1’(‘0’) transitions to suspend (fast start-up) state
wakeup_int: ‘1’(‘0’) triggers an interrupt, when a gyro wakeup is triggered

3.10.22 Register (0x6D) SELF_TEST

ADDRESS 0x6D
RESET 0b0000-0000
MODE RW
DESCRIPTION Contains the settings for the sensor self-test configuration and trigger.
DEFINITION

Name		**Register (0x6D) SELF_TEST**		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	Reserved			gyr_self_test_ enable

Bit	**3**	**2**	**1**	**0**
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	Reserved	Reserved	Reserved	Reserved

reserved: write ‘0x0’

gyr_self_test_enable: starts self-test of the gyroscope. The result can be obtained from Register (0x1B) STATUS.

3.10.23 Register (0x70) NV_CONF

ADDRESS 0x70
RESET 0x00
MODE RW
DESCRIPTION Contains settings for the digital interface.
DEFINITION

This register is backed by NVM and loaded from NVM during boot-up.

Name		**Register (0x70) NV_CONF**		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	Reserved			
Bit	**3**	**2**	**1**	**0**
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	reserved	i2c_wdt_en	i2c_wdt_sel	spi_en

reserved: write ‘0’

i2c_wdt_en: if I²C interface mode is selected then ‘1´ → enable, or ‘0’ → disables the watchdog at the SDI pin (= SDA for I²C)

i2c_wdt_sel: select an I²C watchdog timer period of ‘0’ → 1 ms, or ‘1’ → 50 ms

spi_en: disable the I²C and only enable SPI for the interface, when it is in autoconfig if_mode.

3.10.24 Register (0x74-0x77) OFFSET

ADDRESS 0x74 (4 byte)
RESET Reads from NVM
MODE RW
DESCRIPTION Contains the offset compensation values for the gyroscope
DEFINITION
Offset values, which are added to the internal filtered and pre-filtered data for the sensor if the function is enabled with gyr_off_en in the register; the offset values are represented with two's complement notation; the content of the register may be written to the NVM; it is automatically restored from the NVM after each power-on or soft reset; offset values may be written directly by the user; it is generated automatically after triggering the fast offset compensation procedure.

[3]	**off_gyr_x<7:0>**
[4]	off_gyr_y<7:0>
[5]	off_gyr_z<7:0>

Name		**Register (0x77) OFFSET [6]**		
Bit	7		5	4
Read/Write	R/W		R/W	R/W
Reset Value	0		0	0
Content	gyr_off_en		off_gyr_z<9:8>	

Bit	**3**	**2**	**1**	**0**
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	off_gyr_y<9:8>		off_gyr_x<9:8>	

The offset of the gyroscope off_gyr_[xyz] is a two-complement number in units of 0.12 deg/s*$2^{Val(gyr\_range\_off)}$, i.e. the resolution may be configured from 0.12 to 0.98 deg/s and the range from 31.25 to 250 deg/s. The configuration is done in the Register (0x70) NV_CONF.

The MSBs for the gyro offset setting are also contained in OFFSET[6]. Aside from this, the register also contains the two bits gyr_off_en, which can be set to 1 in order to enable gyro offset compensation.

3.10.25 Register (0x7E) CMD

Register (0x7E) CMD
ADDRESS 0x7E
RESET 0x00
MODE W
DESCRIPTION Command register triggers operations like *softreset*, NVM programming, etc.
DEFINITION

Name				
Bit	7	6	5	4
Read/Write	W	W	W	W
Reset Value	0	0	0	0
Content	cmd<7:4>			
Bit	**3**	**2**	**1**	**0**
Read/Write	W	W	W	W
Reset Value	0	0	0	0
Content	cmd<3:0>			

During the time a command is executed, it occupies the Register (0x7E) CMD. All new writes to this register are dropped during this time with the exception of the softreset command. If a write to the Register (0x7E) CMD is dropped, drop_cmd_err in Register (0x02) ERR_REG is set.

Table 24: Typical and max. execution times for which the CMD register is occupied

Description	Command code	Typ. time in ms	Max. time in ms
Set PMU mode of gyroscope to normal or fast start-up from suspend mode	0x15; 0x17	55	80

The time it takes to perform a soft reset in conjunction with re-starting a sensor is essentially given by the corresponding PMU command execution time in Table 24 (to be more exact, a system start-up time of 300 µs has to be added to the times given for PMU switching).

cmd:

start_foc: 0x03
Starts Fast Offset Calibration as configured in Register (0x69) FOC_CONF and stores the result into the Register (0x74-0x77) OFFSET register.

gyr_set_pmu_mode: 0b0001 01nn
Sets the PMU mode for the gyroscope. The encoding for 'nn' is identical to gyr_pmu_status in Register (0x03) PMU_STATUS

0x10	tmp_susp	Sets the PMU mode to suspend.
0x11	tmp_norm	Sets the PMU mode to normal. This command is necessary if user want to program NVM.

0x14	gyr_susp	Sets the PMU mode for the Gyroscope to suspend.
0x15	gyr_norm	Sets the PMU mode for the Gyroscope to normal.
0x16	gyr_res	Reserved
0x17	gyr_fsup	Sets the PMU mode for the Gyroscope to fast start-up.

prog_nvm: 0xA0

Writes the NVM backed registers into NVM.

fifo_flush: 0xB0

clears all data in the FIFO, does not change the Register (0x46-0x47) FIFO_CONFIG and Register (0x45) FIFO_DOWNS registers.

softreset: 0xB6

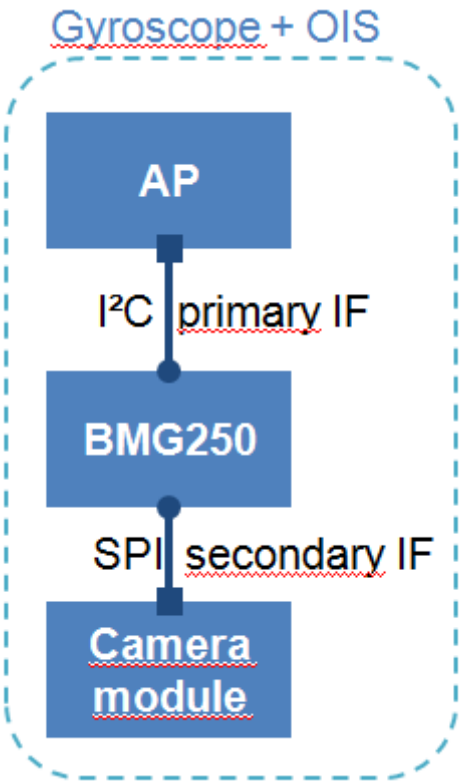
triggers a reset including a reboot. Other values are ignored. Following a delay, all user configuration settings are overwritten with their default state or the setting stored in the NVM, wherever applicable. This register is functional in all operation modes.

4. Digital interfaces

4.1 Interface

Beside the standard primary interface (I²C and SPI configurable), where the sensor acts as a slave to the application processor, BMG250 supports a secondary OIS-Interface (SPI).

In this mode, the secondary interface can be used as an OIS-Interface to be connected to an external OIS-Control unit, where the OIS controller will act as a master and the BMG250 as a slave.



By default, the BMG250 operates in I²C mode. The BMG250 interface can also be configured to operate in a SPI 4-wire configuration. It can be re-configured by software to work in 3-wire mode instead of 4-wire mode.

The mapping for the interface of the BMG250 is given in the following table:

Table 25: Mapping of the interface pins

Pin#	Name	I/O Type	Description	Connect to		
				in SPI4W	in SPI3 W	in I²C
1	SDO	Digital I/O	Serial data output in SPI Address select in I²C mode	MISO	DNC (float)	SA0 (GND for default addr.)
4	INT1	Digital I/O	Interrupt pin 1 *)	INT1	INT1	INT1
9	INT2	Digital I/O	Interrupt pin 2 *)	INT2	INT2	INT2
12	CSB	Digital in	Chip select for SPI mode / Protocol selection pin	CSB	CSB	VDDIO
13	SCx	Digital in	SCK for SPI serial clock SCL for I²C serial clock	SCK	SCK	SCL
14	SDx	Digital I/O	SDA serial data I/O in I²C SDI serial data input in SPI 4W SDA serial data I/O in SPI 3W	MOSI	SISO	SDA

The following table shows the electrical specifications of the interface pins:

Table 26: Electrical specification of the interface pins

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pull-up Resistance, CSB pin	R_{up}	Internal Pull-up Resistance to VDDIO	75	100	150	kΩ
Input Capacitance	C_{in}				5	pF
I²C Bus Load Capacitance (max. drive capability)	C_{I2C_Load}				400	pF

4.1.1 Interface I²C/SPI Protocol Selection

The protocol is automatically selected based on the chip select CSB pin behavior after power-up. At reset / power-up, BMG250 is in I²C mode. If CSB is connected to V_{DDIO} during power-up and not changed the sensor interface works in I²C mode. For using I²C, it is recommended to hard-wire the CSB line to V_{DDIO}. Since power-on-reset is only executed when, both V_{DD} and V_{DDIO} are established, there is no risk of incorrect protocol detection due to power-up sequence.
If CSB sees a rising edge after power-up, the BMG250 interface switches to SPI until a reset or the next power-up occurs. Therefore, a CSB rising edge is needed before starting the SPI

communication. Hence, it is recommended to perform a SPI single read access to the ADDRESS 0x7F before the actual communication is started in order to use the SPI interface.
If toggling of the CSB bit is not possible without data communication, there is in addition the *spi_en* bit in Register (0x70) NV_CONF, which can be used to permanently set the interface to SPI without the need to toggle the CSB pin at every power-up or reset.

4.1.2 SPI Interface

The timing specification for SPI of the BMG250 is given in the following table:

Table 27: SPI timing, valid at $V_{DDIO} \geq 1.71V$, if not stated otherwise

Parameter	Symbol	Condition	Min	Max	Units
Clock Frequency	f_{SPI}	Max. Load on SDI or SDO = 25pF, $V_{DDIO} \geq 1.71$ V		10	MHz
		$V_{DDIO} < 1.71V$		7.5	MHz
SCK Low Pulse	t_{SCKL}		48		ns
SCK High Pulse	t_{SCKH}		48		ns
SDI Setup Time	t_{SDI_setup}		20		ns
SDI Hold Time	t_{SDI_hold}		20		ns
SDO Output Delay	t_{SDO_OD}	Load = 30pF, $V_{DDIO} \geq 1.62V$	45		ns
		Load = 25pF, $V_{DDIO} < 1.62V$	52		ns
		Load = 250pF, $V_{DDIO} > 2.4V$	45		ns
CSB Setup Time	t_{CSB_setup}		20		ns
CSB Hold Time	t_{CSB_hold}		40		ns
Idle time between write accesses, normal mode	$t_{IDLE\_wacc\_nm}$		2		µs
Idle time between write accesses, suspend mode	$t_{IDLE\_wacc\_sum}$		450		µs

The following figure shows the definition of the SPI timings:

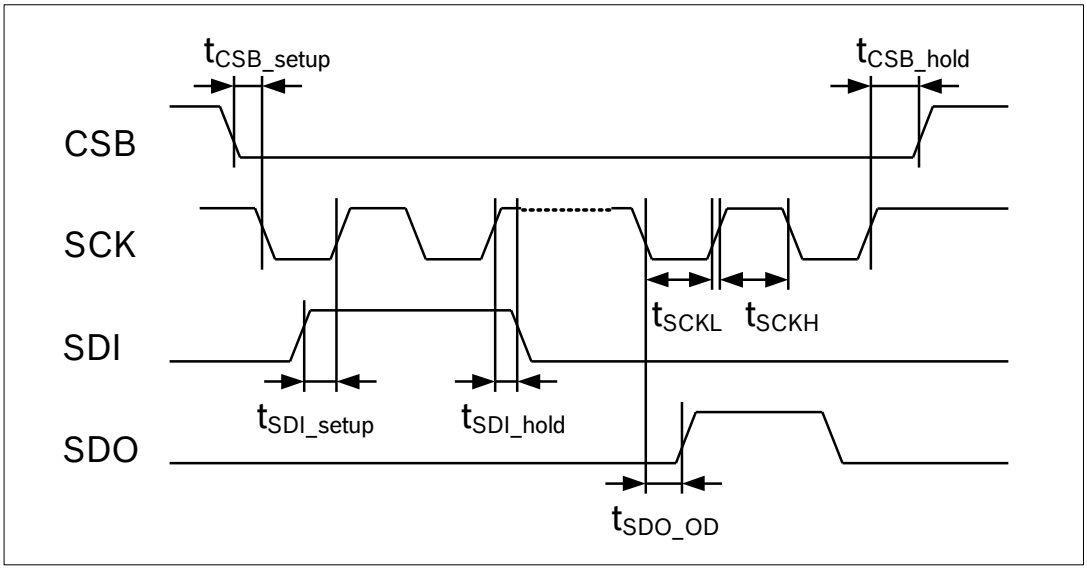


Figure 22: SPI timing diagram

The SPI interface of the BMG250 is compatible with two modes, ´00´ [CPOL = ´0´ and CPHA = ´0´] and ´11´ [CPOL = ´1´ and CPHA = ´1´]. The automatic selection between ´00´ and ´11´ is controlled based on the value of SCK after a falling edge of CSB.

Two configurations of the SPI interface are supported by the BMG250: 4-wire and 3-wire. The same protocol is used by both configurations. The device operates in 4-wire configuration by default. It can be switched to 3-wire configuration by writing ´1´ to Register (0x6B) IF_CONF *spi3*. Pin SDI is used as the common data pin in 3-wire configuration.
For single byte read as well as write operations, 16-bit protocols are used. The BMG250 also supports multiple-byte read and write operations.

In SPI 4-wire configuration CSB (chip select low active), SCK (serial clock), SDI (serial data input), and SDO (serial data output) pins are used. The communication starts when the CSB is pulled low by the SPI master and stops when CSB is pulled high. SCK is also controlled by SPI master. SDI and SDO are driven at the falling edge of SCK and should be captured at the rising edge of SCK.

The basic write operation waveform for 4-wire configuration is depicted in the following figure. During the entire write cycle SDO remains in high-impedance state.

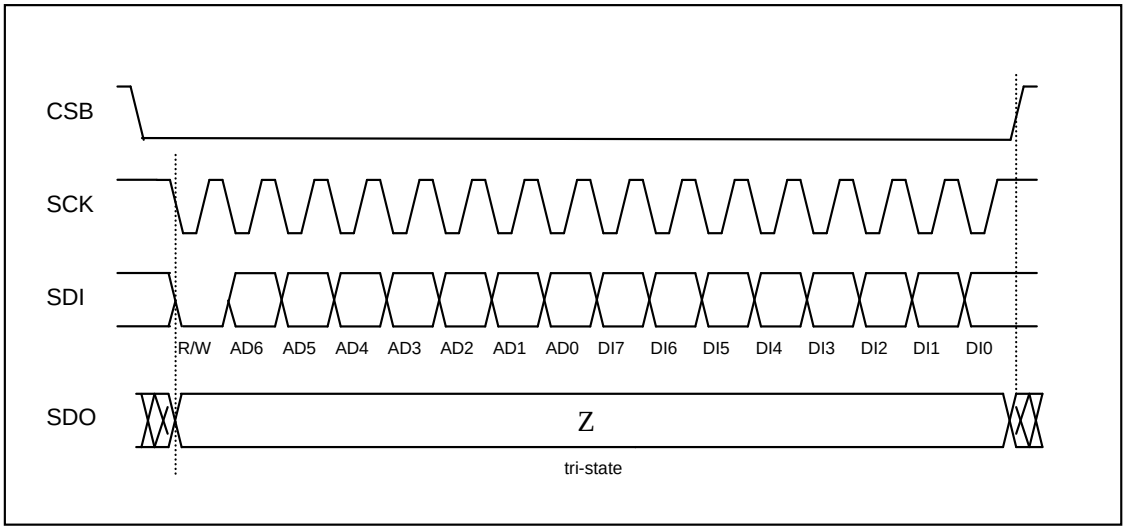


Figure 23: 4-wire basic SPI write sequence (mode ´11´)

The basic read operation waveform for 4-wire configuration is depicted in the figure below:

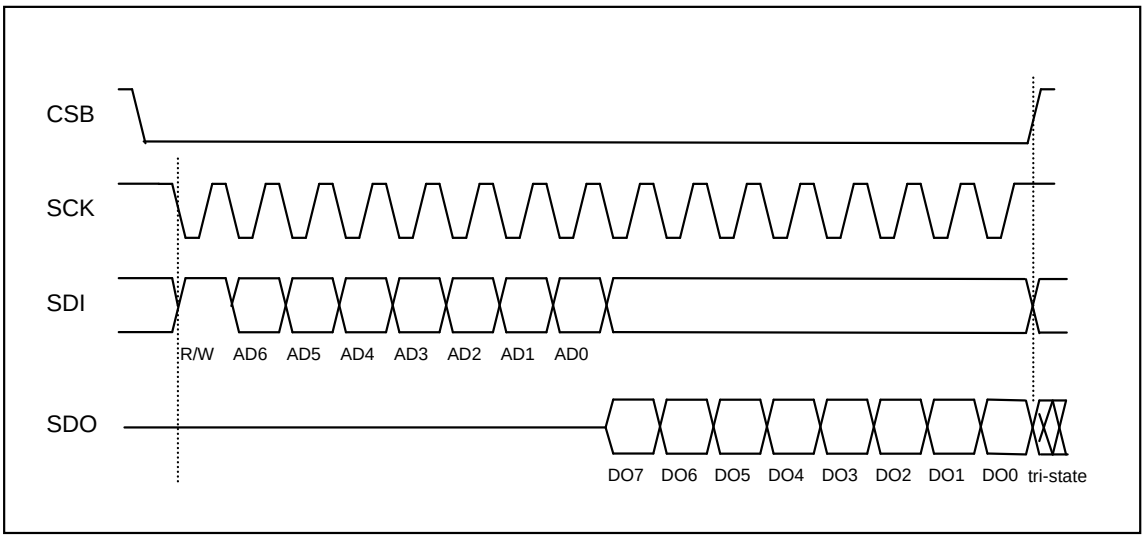


Figure 24: 4-wire basic SPI read sequence (mode ´11´)

The data bits are used as follows:

Bit0: Read/Write bit. When 0, the data SDI is written into the chip. When 1, the data SDO from the chip is read.

Bit1-7: Address AD(6:0).

Bit8-15: when in write mode, these are the data SDI, which will be written into the address. When in read mode, these are the data SDO, which are read from the address.

Multiple read operations are possible by keeping CSB low and continuing the data transfer. Only the first register address has to be written. Addresses are automatically incremented after each read access as long as CSB stays active low.

The principle of multiple read is shown in figure below:

	Control byte		Data byte	Data byte	Data byte	
Start	RW	Register adress (02h)	Data register - adress 02h	Data register - adress 03h	Data register - adress 04h	Stop
CSB = 0	1	0 0 0 0 0 1 0	X X X X X X X X	X X X X X X X X	X X X X X X X X	CSB = 1

Figure 25: SPI multiple read

In SPI 3-wire configuration CSB (chip select low active), SCK (serial clock), and SDI (serial data input and output) pins are used. While SCK is high, the communication starts when the CSB is pulled low by the SPI master and stops when CSB is pulled high. SCK is also controlled by SPI master. SDI is driven (when used as input of the device) at the falling edge of SCK and should be captured (when used as the output of the device) at the rising edge of SCK.

The protocol as such is the same in 3-wire configuration as it is in 4-wire configuration. The basic operation wave-form (read or write access) for 3-wire configuration is depicted in the figure below:

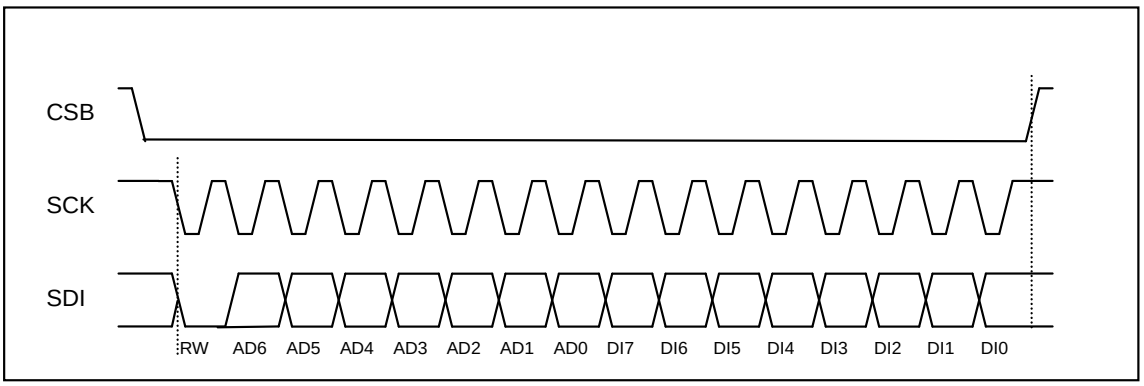


Figure 26: 3-wire basic SPI read or write sequence (mode ´11´)

4.1.3 I²C Interface

The I²C bus uses SCL (= SCx pin, serial clock) and SDA (= SDx pin, serial data input and output) signal lines. Both lines are connected to V_{DDIO} externally via pull-up resistors so that they are pulled high when the bus is free.

The I²C addresses are identical to BMG160. The default I²C address of the device is 0b1101000 (0x68). It is used if the SDO pin is pulled to ´GND´. The alternative address 0b1101001 (0x69) is selected by pulling the SDO pin to ´VDDIO´.

The I²C interface of the BMG250 is compatible with the I²C Specification UM10204 Rev. 03 (19 June 2007), available at http://www.nxp.com. The BMG250 supports **I²C standard mode and fast mode**, only 7-bit address mode is supported. For V_{DDIO} = 1.2V to 1.62 V the guaranteed voltage output levels are slightly relaxed as described in Table 1 of the electrical specification section.

BMG250 also supports an **extended I²C mode** that allows using clock frequencies up to 1 MHz. In this mode all timings of the fast mode apply and it additionally supports clock frequencies up to 1MHz.

The timing specification for I²C of the BMG250 is given in the following table:

Table 28: I²C timings

Parameter	Symbol	Condition	Min	Max	Units
Clock Frequency	f_{SCL}			1000	kHz
SCL Low Period	t_{LOW}		1.3		µs
SCL High Period	t_{HIGH}		0.6		
SDA Setup Time	t_{SUDAT}		0.1		
SDA Hold Time	t_{HDDAT}		0.0		
Setup Time for a repeated Start Condition	t_{SUSTA}		0.6		
Hold Time for a Start Condition	t_{HDSTA}		0.6		
Setup Time for a Stop Condition	t_{SUSTO}		0.6		
Time before a new Transmission can start	t_{BUF}	suspend mode	400		
		normal mode	1.3		
Idle time between write accesses, normal mode, suspend mode	$t_{IDLE\_wacc\_nm}$	suspend mode	400		
		normal mode	1.3		
Idle time between write accesses, suspend mode, suspend mode	$t_{IDLE\_wacc\_sum}$		400		

The figure below shows the definition of the I²C timings given in Table 28:

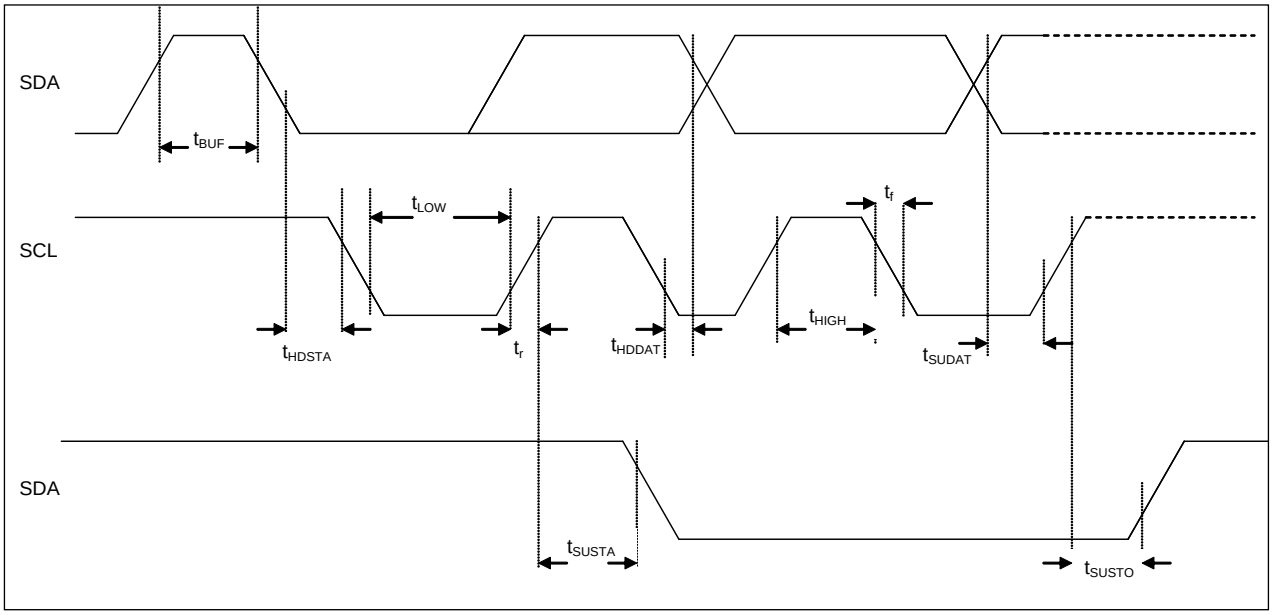


Figure 27: I²C timing diagram

The I²C protocol works as follows:

START: Data transmission on the bus begins with a high to low transition on the SDA line while SCL is held high (start condition (S) indicated by I²C bus master). Once the START signal is transferred by the master, the bus is considered busy.

STOP: Each data transfer should be terminated by a Stop signal (P) generated by master. The STOP condition is a low to HIGH transition on SDA line while SCL is held high.

ACKS: Each byte of data transferred must be acknowledged. It is indicated by an acknowledge bit sent by the receiver. The transmitter must release the SDA line (no pull down) during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.

In the following diagrams these abbreviations are used:

S	Start
P	Stop
ACKS	Acknowledge by slave
ACKM	Acknowledge by master
NACKM	Not acknowledge by master
RW	Read / Write

A START immediately followed by a STOP (without SCL toggling from ´VDDIO´ to ´GND´) is not supported. If such a combination occurs, the STOP is not recognized by the device.

I²C write access:
I²C write access can be used to write a data byte in one sequence.

The sequence begins with start condition generated by the master, followed by 7 bits slave address and a write bit (RW = 0). The slave sends an acknowledge bit (ACKS = 0) and releases the bus. Then the master sends the one byte register address. The slave again acknowledges the transmission and waits for the 8 bits of data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol.

Example of an I²C write access:

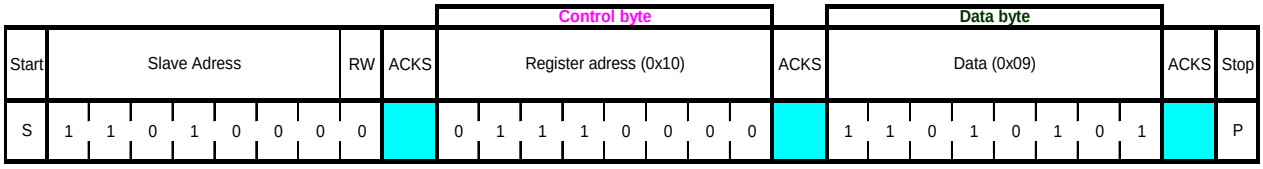


Figure 28: I²C write

I²C read access:
I²C read access also can be used to read one or multiple data bytes in one sequence.

A read sequence consists of a one-byte I²C write phase followed by the I²C read phase. The two parts of the transmission must be separated by a repeated start condition (S). The I²C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, the master generates again a start condition and sends the slave address together with a read bit (RW = 1). Then the master releases the bus and waits for the data bytes to be read out from slave. After each data byte the master has to generate an acknowledge bit (ACKS = 0) to enable further data transfer. A NACKM (ACKS = 1) from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a STOP condition and terminate the transmission.
The register address is automatically incremented and, therefore, more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified since the latest I²C write command. By default the start address is set at 0x00. In this way repetitive multi-bytes reads from the same starting address are possible.

In order to prevent the I²C slave of the device to lock-up the I²C bus, a watchdog timer (WDT) is implemented. The WDT observes internal I²C signals and resets the I²C interface if the bus is locked-up by the BMG250. The activity and the timer period of the WDT can be configured through the bits *i2c_wdt_en* and *i2c_wdt_sel* at Register (0x70) NV_CONF.

Writing ´1´ (´0´) to Register (0x70) NV_CONF *i2c_wdt_en* activates (de-activates) the WDT. Writing ´0´ (´1´) to Register (0x70) NV_CONF *i2c_wdt_en* selects a timer period of 1 ms (50 ms).

Example of an I²C read access (reading gyro data):

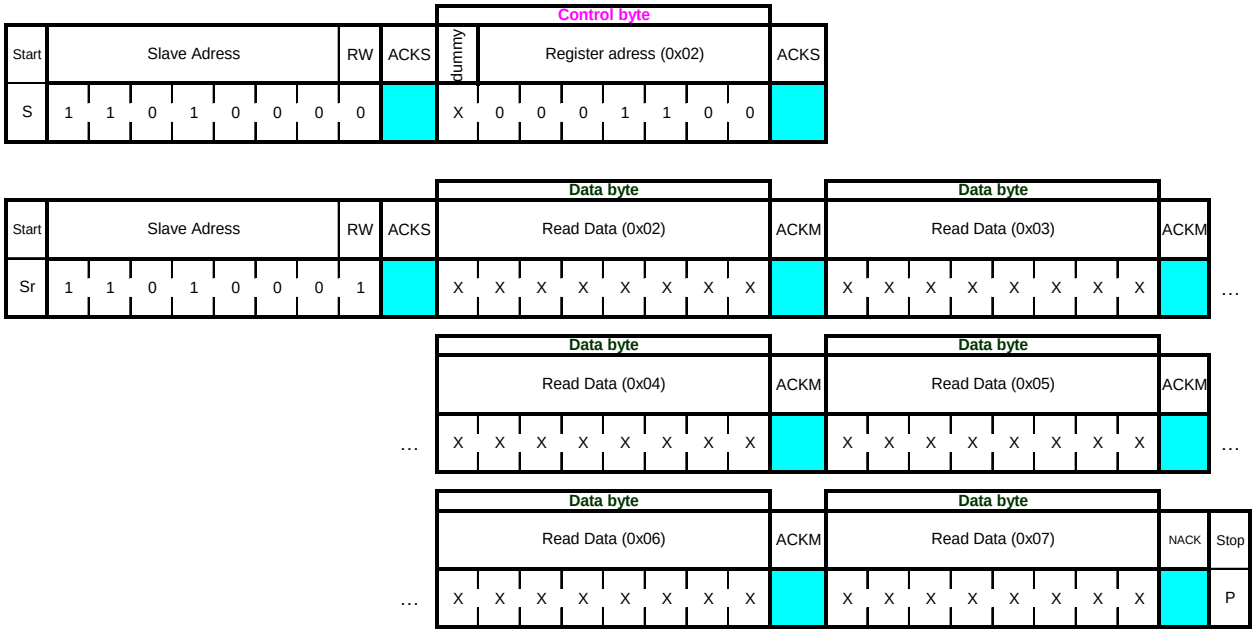


Figure 29: I²C multiple read

4.1.4 SPI and I²C Access Restrictions

In order to allow for the correct internal synchronization of data written to the BMG250, certain access restrictions apply for consecutive write accesses or a write/read sequence through the SPI as well as I²C interface. The required waiting period depends on whether the device is operating in normal mode or other modes.

As illustrated in the figure below, an interface idle time of at least 2 µs is required following a write operation when the device operates in normal mode. In suspend mode an interface idle time of least 450 µs is required[1].

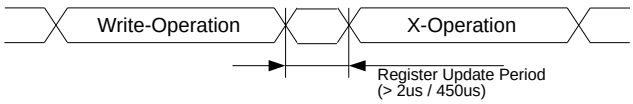


Figure 30: Post-Write Access Timing Constraints

[1] The times are preliminary and need to be verified.

4.2 Secondary Interface

OIS Interface (SPI) for connecting to a OIS control unit:
Secondary interface for OIS application can be enabled by writing '01' to Register (0x6B) IF_CONF *if_mode*.
In this case the secondary interface is used as a SPI interface where an external control unit is connected as a master to BMG250. The external control unit can be e.g. an OIS controller.
If secondary interface is used, primary interface is limited to I²C mode.
The mapping for the secondary interface of the BMG250 is given in the following table:

Table 29: Mapping of the secondary interface pins

Pin#	Name	I/O Type	Description	Connect to (secondary IF)		
				in SPI4W	in SPI3W	in I²C
10	OSCB	Digital I/O	Secondary OIS interface	CSB	CSB	DNC
11	OSDO	Digital I/O	Secondary OIS interface	MISO	DNC	DNC

4.2.1 Camera module connected to secondary interface for OIS

BMG250 supports specific optical image stabilization (OIS) applications with a dedicated interface. This interface is used for direct access to pre-filtered gyroscope data with minimum latency. Pre-filtered gyroscope data is available at output data rate (ODR) of 6.4 kHz and can be read out via OIS SPI interface at 10MHz maximum speed.
The OIS SPI interface supports 3-wire SPI as well as 4-wire SPI.

The timings of the secondary SPI interface are the same as for the primary SPI interface, see chapter 4.1.2. The connection diagrams are depicted in chapter.

5. Pin-out and Connection diagrams

5.1 Pin-out BMG250

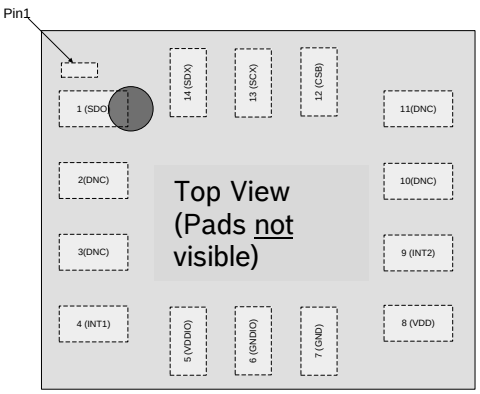


Figure 31: Pin-out top view

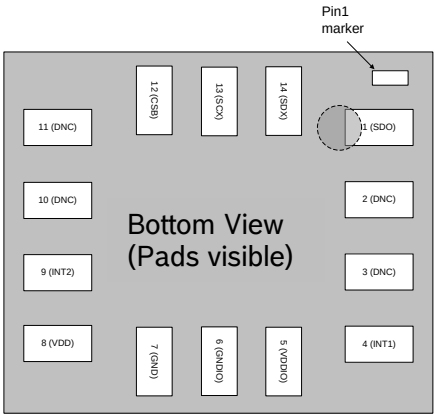


Figure 32: Pin-out bottom view

Table 30: BMG250 Pin-out and pin connections are described in the table below

Pin#	Name	I/O Type	Description
1	SDO	Digital I/O	Serial data output in SPI Address select in I²C mode
2	ASDx	Digital I/O	MOSI serial data input in SPI 4W 2ndary Interface SISO serial data I/O in SPI 3W 2ndary Interface Other configuration: Do not connect (or GND)
3	ASCx	Digital in	SPI serial clock for 2ndary Interface Other configuration: Do not connect (or GND)
4	INT1	Digital I/O	Interrupt pin 1 *)
5	VDDIO	Supply	Digital I/O supply voltage (1.2 ... 3.6V)
6	GNDIO	Ground	Ground for I/O
7	GND	Ground	Ground for digital & analog
8	VDD	Supply	Power supply analog & digital domain (1.62V – 3.6V)
9	INT2	Digital I/O	Interrupt pin 2 *)
10	OSCB	Digital I/O	CSB in SPI as 2ndary Interface Other configuration: Do not connect (or GND)
11	OSCO	Digital I/O	MISO in SPI 4W 2ndary Interface Other configuration: Do not connect (or GND)
12	CSB	Digital in	Chip select for SPI mode / Protocol selection pin
13	SCx	Digital in	SCK for SPI serial clock SCL for I²C serial clock
14	SDx	Digital I/O	SDA serial data I/O in I²C MOSI serial data input in SPI 4W (without 2ndary Interface) SISO serial data I/O in SPI 3W (without 2ndary Interface)

*) If INT1 and/or INT2 are not used, please do not connect them (DNC)

NOTE: all pins must be soldered to the PCB even if they are electrically not connected

5.2 Connection diagrams

5.2.1 I²C interface without using secondary OIS interface

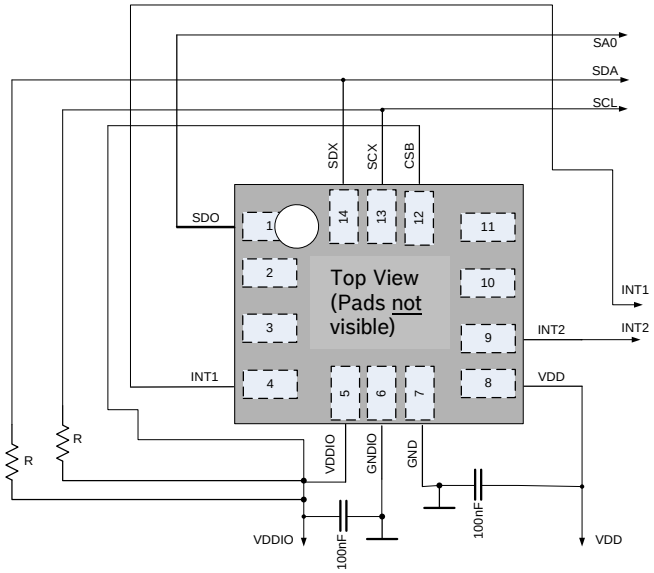


Figure 33: I²C as interface

5.2.2 SPI 3-wire interface without using secondary OIS interface

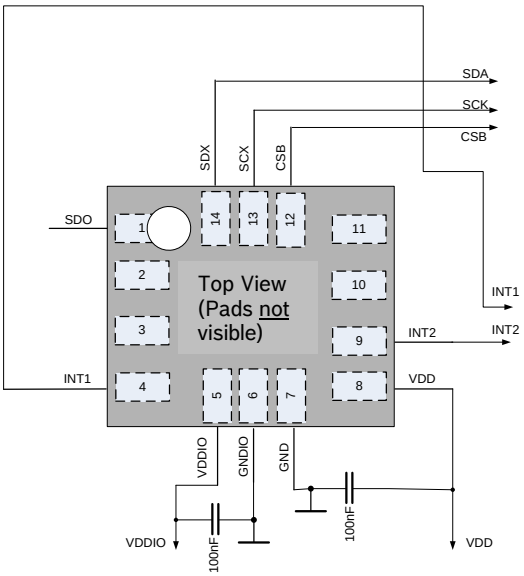


Figure 34: Only SPI 3-wire as interface

5.2.3 SPI 4-wire interface without using secondary OIS interface

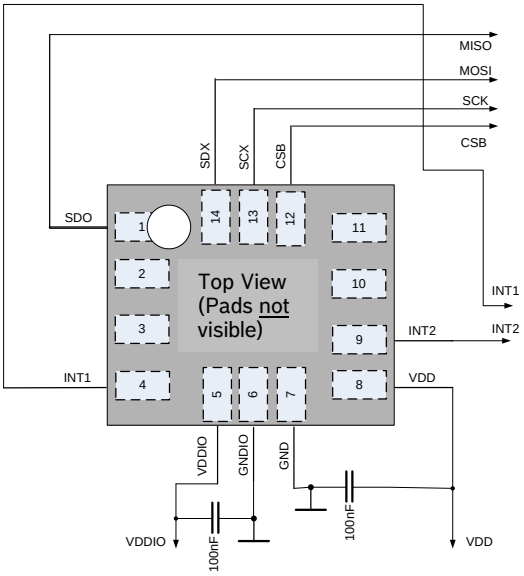
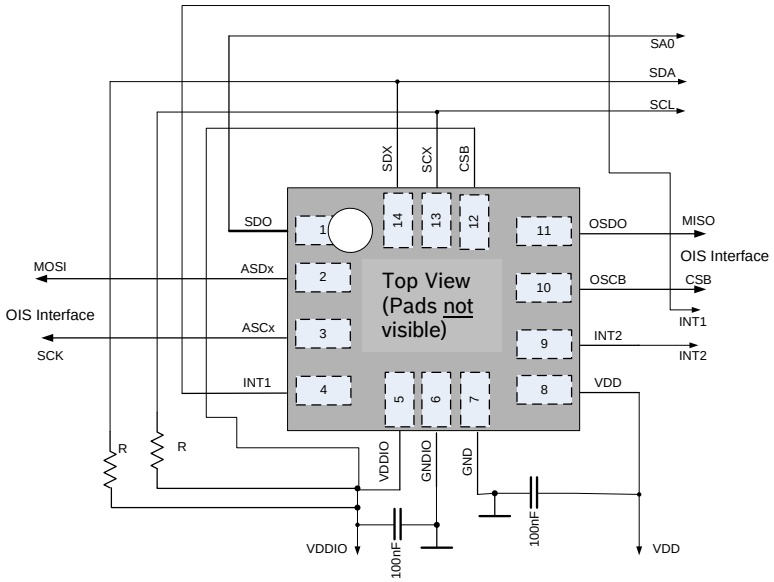


Figure 35: Only SPI 4-wire as interface

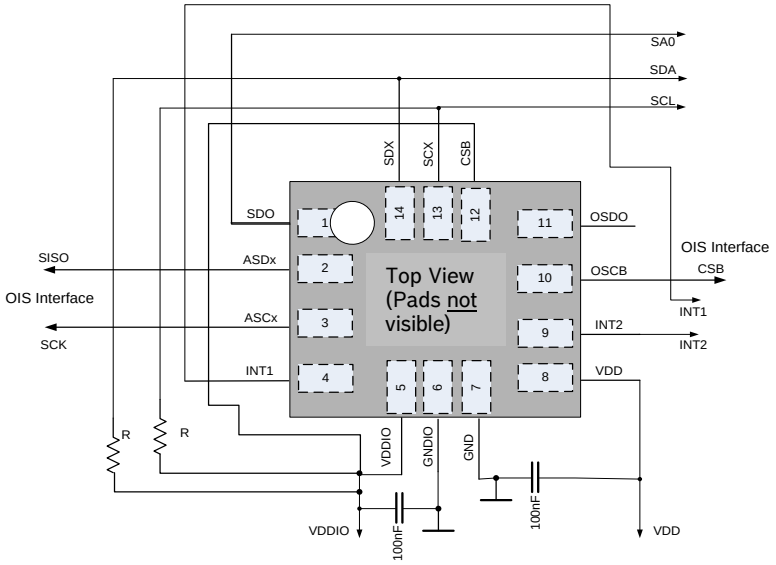
5.2.4 Primary I²C and secondary 4-wire SPI as OIS interface

Figure 36: Using I²C and 4-wire SPI as OIS interface



5.2.5 Primary I²C and secondary 3-wire SPI as OIS interface

Figure 37: Using I²C and 3-wire SPI as OIS interface



6. Package

6.1 Outline Dimensions

The package dimension is LGA 2.5mm x 3.0mm x 0.83mm.
Unit of the following drawing is mm. Note: Unless otherwise specified tolerance = decimal ±0.05 mm.

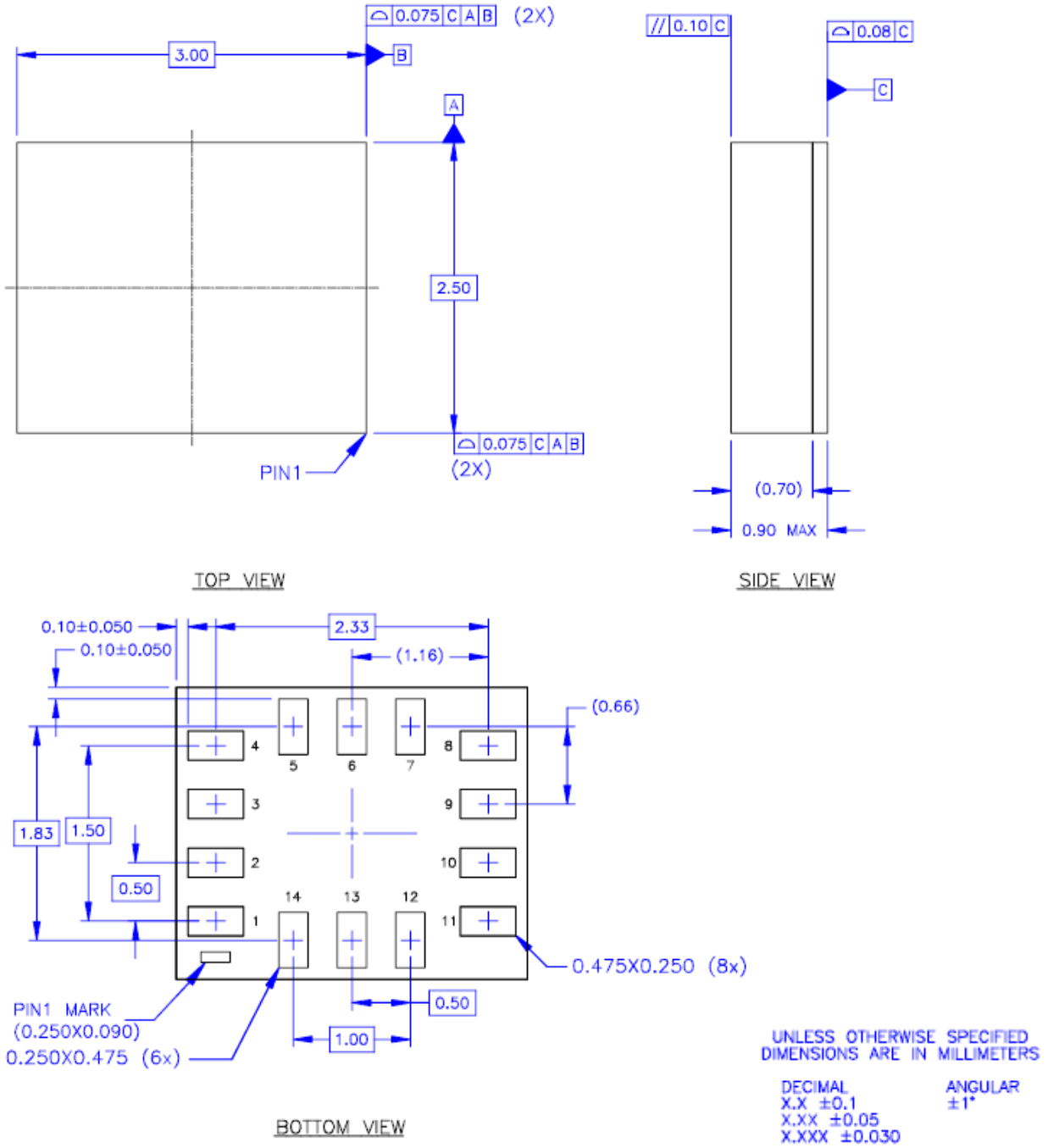


Figure 38: Packaging outline dimensions

Note: Pin1 marker is internally connected to Pin1. It must not be connected to a different signal than Pin1.

6.2 Sensing axes orientation

If the sensor is rotated in the indicated directions, the corresponding channels of the device will deliver a positive yaw rate signal. If the sensor is at rest without any rotation the output of the corresponding gyroscope channel will be “zero” (static acceleration).

Example: If the sensor would be placed on a seconds hand of a watch with the arrows of the following Fig. pointing towards the watch’s dial, the output signals are:

- + 6°/sec for the Ω_X GYR channel
- + 6°/sec for the Ω_Y GYR channel
- + 6°/sec for the Ω_Z GYR channel

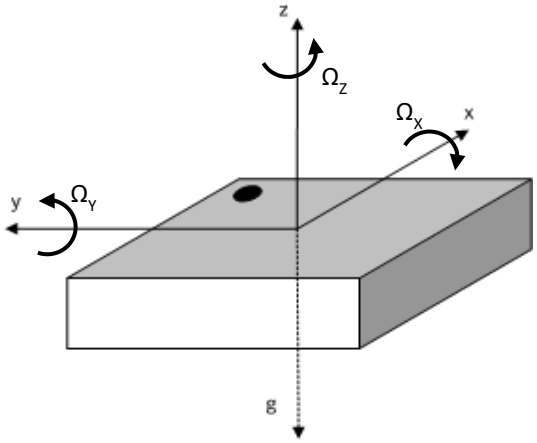


Figure 39: definition of sensing axes orientation

For reference the figure below shows the Android device orientation with an integrated BMG250.

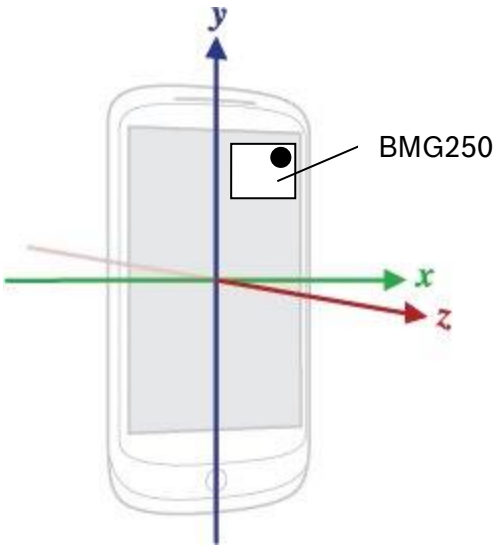


Figure 40: Android axis definition with BMG250

6.3 Landing pattern recommendation

The following landing pad recommendation is given for maximum stability of the solder connections.

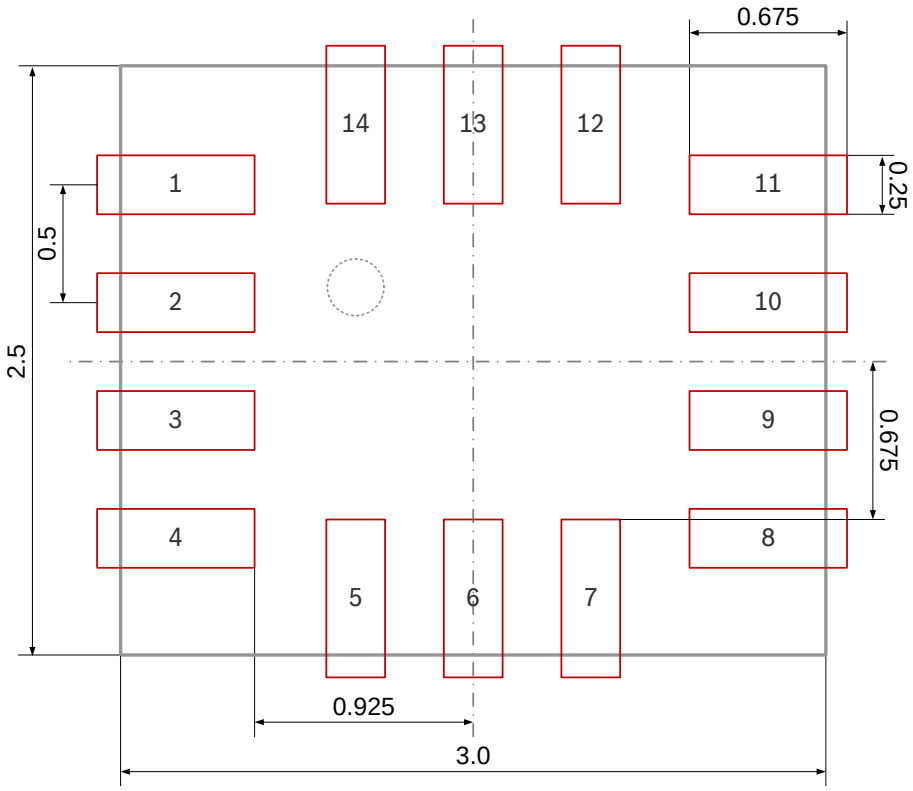


Figure 41: Landing pattern recommendation for BMG250

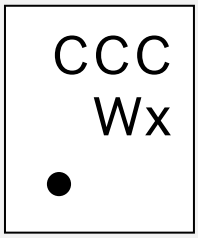
Note: Pin1 marker is internally connected to Pin1. It must not be connected to a different signal than Pin1.

The size of the landing pads may be further reduced in order to minimize solder-stress induced effects if sufficient control over the soldering process is given. Please contact your sales representative for further details.

6.4 Marking

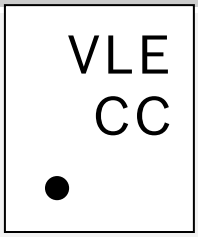
6.4.1 Mass production marking

Table 31: Marking of mass samples

Labeling	Name	Symbol	Remark
	Counter ID	CCC	3 alphanumeric digits, variable to generate trace-code
	First letter of second row	W	Product identifier W, denoting BMG250
	Second letter of second row	x	Internal use – various digits possible
	Pin 1 identifier	●	--

6.4.2 Engineering samples

Table 32: Marking of engineering samples

Labeling	Name	Symbol	Remark
	Internal ID	VLE	Various digits – internal “E” denotes engineering status
	Second row	CC	CC - internal revision ID
	Pin 1 identifier	●	--

6.5 Soldering guidelines

The moisture sensitivity level of the BMG250 sensors corresponds to JEDEC Level 1, see also

- IPC/JEDEC J-STD-020C "Joint Industry Standard: Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices"
- IPC/JEDEC J-STD-033A "Joint Industry Standard: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices"

The sensor fulfils the lead-free soldering requirements of the above-mentioned IPC/JEDEC standard, i.e. reflow soldering with a peak temperature up to 260°C.

Profile Feature		Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)		3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})		150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)		217 °C 60-150 seconds
Peak/Classification Temperature (Tp)		260 °C
Time within 5 °C of actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate		6 °C/second max.
Time 25 °C to Peak Temperature		8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

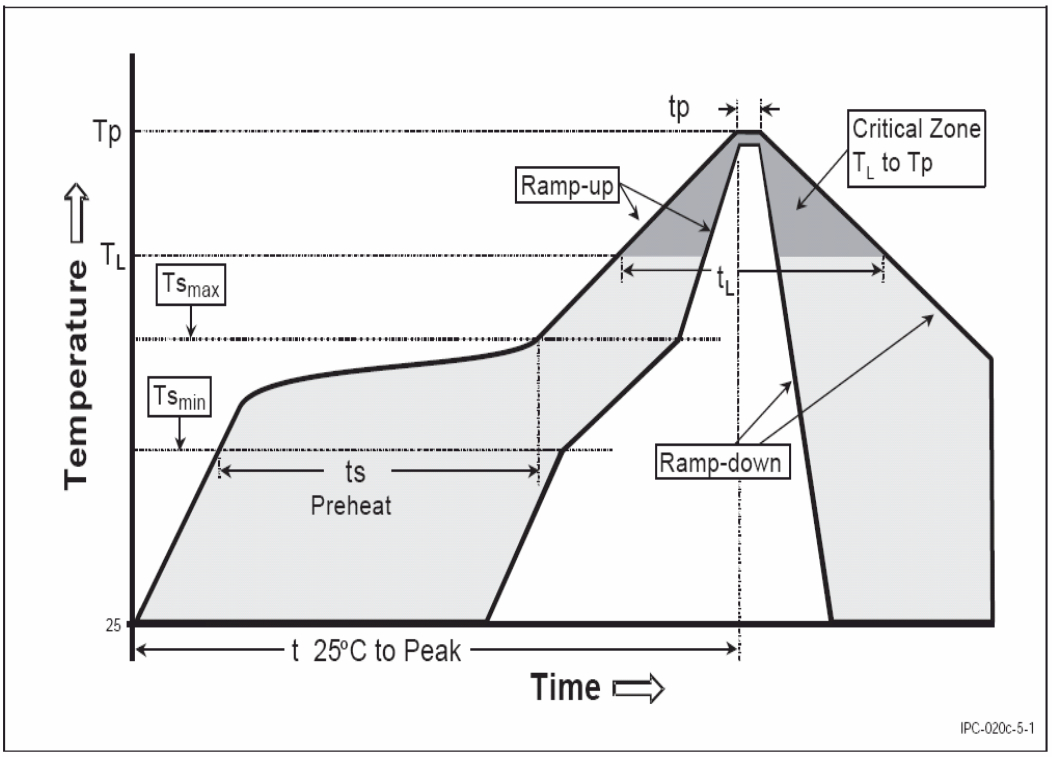


Figure 42: Soldering profile

6.6 Handling instructions

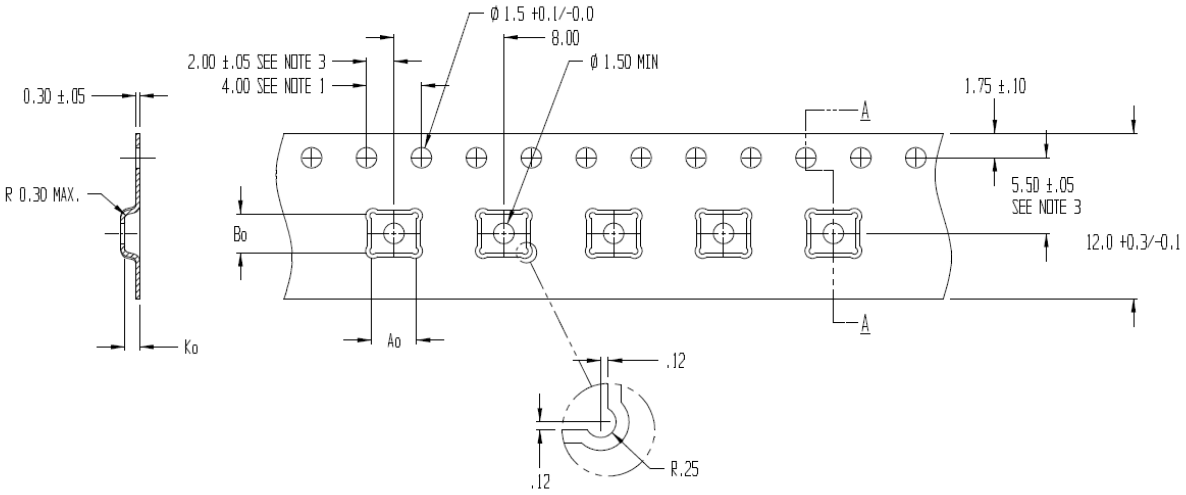
Micromechanical sensors are designed to sense rotations with high accuracy even at low turn rates and contain highly sensitive structures inside the sensor element. The MEMS sensor can tolerate mechanical shocks up to several thousand g's. However, these limits might be exceeded in conditions with extreme shock loads such as e.g. hammer blow on or next to the sensor, dropping of the sensor onto hard surfaces etc.

We recommend to avoid g-forces beyond the specified limits during transport, handling and mounting of the sensors in a defined and qualified installation process.

This device has built-in protections against high electrostatic discharges or electric fields (e.g. 2kV HBM); however, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

6.7 Tape and reel specification

The BMG250 is shipped in a standard cardboard box.
The box dimension for 1 reel is: L × W × H = 35 cm × 35 cm × 6 cm.
BMG250 quantity: 5,000pcs per reel, please handle with care.



A_0 = 3.30, B_0 = 2.80, K_0 = 1.10

Note:

- Tolerances unless noted: ±0.1
- Sprocket hole pitch cumulative tolerance ±0.1
- Camber in compliance with EIA481
- Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole
- A0 and B0 are calculated on a plane at a distance “R” above the bottom of the pocket

Figure 43: Tape and reel dimensions in mm

6.7.1 Orientation within the reel

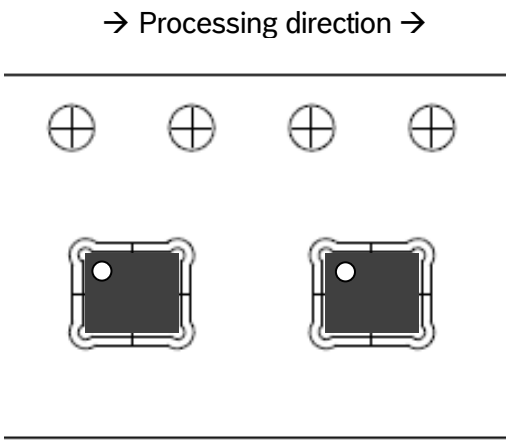


Figure 44: Orientation of the BMG250 devices relative to the tape

6.8 Environmental safety

The BMG250 sensor meets the requirements of the EC restriction of hazardous substances (RoHS) directive, see also:

> *Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.*

6.8.1 Halogen content

The BMG250 is halogen-free. For more details on the analysis results please contact your Bosch Sensortec representative.

6.8.2 Multiple sourcing

Within the scope of Bosch Sensortec's ambition to improve its products and secure the mass product supply, Bosch Sensortec employs multiple sources in the supply chain.

While Bosch Sensortec takes care that all of technical parameters are described above are 100% identical for all sources, there can be differences in device marking and bar code labeling.

However, as secured by the extensive product qualification process of Bosch Sensortec, this has no impact to the usage or to the quality of the product.

7. Legal disclaimer

7.1 Engineering samples

Engineering Samples are marked with an asterisk (*), (E) or (e). Samples may vary from the valid technical specifications of the product series contained in this data sheet. They are therefore not intended or fit for resale to third parties or for use in end products. Their sole purpose is internal client testing. The testing of an engineering sample may in no way replace the testing of a product series. Bosch Sensortec assumes no liability for the use of engineering samples. The Purchaser shall indemnify Bosch Sensortec from all claims arising from the use of engineering samples.

7.2 Product use

Bosch Sensortec products are developed for the consumer goods industry. They may only be used within the parameters of this product data sheet. They are not fit for use in life-sustaining or safety-critical systems. Safety-critical systems are those for which a malfunction is expected to lead to bodily harm, death or severe property damage. In addition, they shall not be used directly or indirectly for military purposes (including but not limited to nuclear, chemical or biological proliferation of weapons or development of missile technology), nuclear power, deep sea or space applications (including but not limited to satellite technology).

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The purchaser accepts the responsibility to monitor the market for the purchased products, particularly with regard to product safety, and to inform Bosch Sensortec without delay of all safety-critical incidents.

7.3 Application examples and hints

With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Bosch Sensortec hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights or copyrights of any third party. The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. They are provided for illustrative purposes only and no evaluation regarding infringement of intellectual property rights or copyrights or regarding functionality, performance or error has been made.

8. Document history and modifications

Rev. No	Chapter	Description of modification/changes	Date
1.0		Initial release	Sept 2015
1.1		Update secondary Interface	May 2016
1.2		Final Release	July 2016
1.3	7	Update of legal disclaimer	Oct 2019
1.4	7	Update of legal disclaimer	Nov 2020

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