ARC EM4 and EM6 Processors

Highlights

- 1.81 DMIPS/MHz
- 4.02 CoreMark/MHz
- 2K–32K instruction/data caches (EM6)
- 512B–2MB instruction and data closely coupled memory (CCM)
- Highly configurable CPU processor core based on next-generation ARCv2 ISA
- Native ARM® AMBA® AHB™ and AHBLite™
- Optional 32x32 or 16x16 single and multi-cycle multiplier
- ECC/Parity support
- Up to 240 interrupts, with up to 16 configurable preemption levels
- Compact JTAG (cJTAG) and JTAG debug interface
- Support for custom instructions

Target Applications

- Storage
  - Memory cards
  - Flash controller
  - SSD controllers
- IoT/Mobile devices
  - Sensors
  - Connectivity
  - Microcontrollers
- Automotive
  - Sensors
  - Controllers
  - ADAS SoCs

32-Bit Processors for Embedded Applications

The DesignWare® ARC® EM4 and EM6 processors are optimized for use in embedded and deeply embedded applications where high performance with minimum power consumption is essential. The cores offer outstanding performance density, delivering 1.81 DMIPS/MHz and 4.02 CoreMark/MHz within a very small footprint and extremely low power consumption.

The ARC EM4 and EM6 processors are based on the ARCv2 instruction set architecture (ISA) and pipeline, which provides leadership power efficiency and code density.

Both the ARC EM4 and EM6 support up to 2MB of closely coupled memory and are ideal for embedded applications in consumer, IoT, networking, automotive and other power- and cost-sensitive applications. The ARC EM6 processor also supports up to 32KB of instruction and data cache.

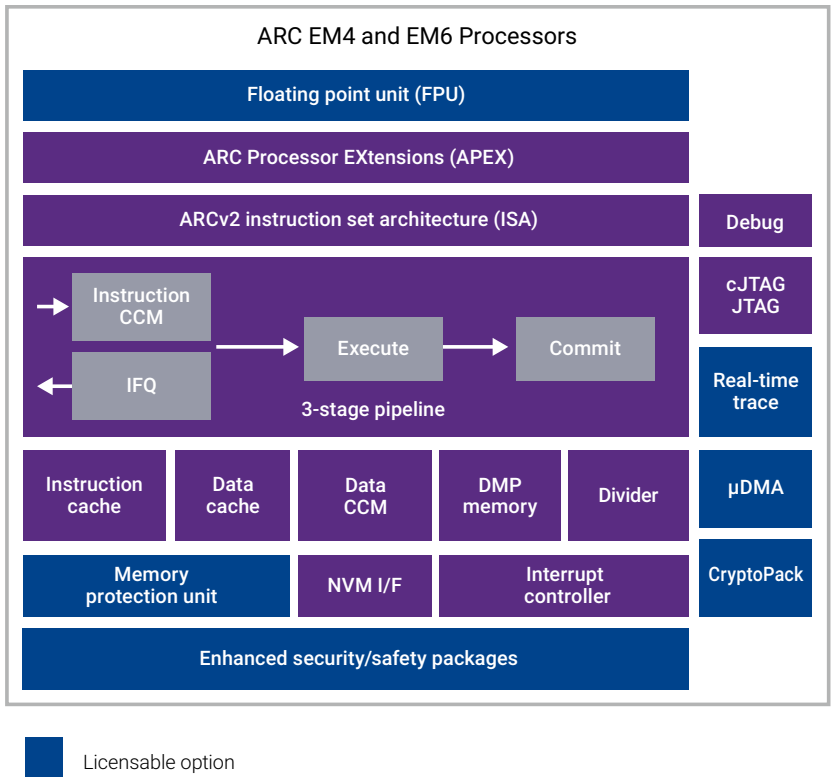

Figure 1: DesignWare ARC EM4 and EM6 block diagram

DesignWare ARCv2 ISA

The ARC EM4 and EM6 processors implement the DesignWare ARCv2 16-/32-bit RISC ISA. The ARCv2 ISA supports advanced processor capabilities and incorporates instructions that improve code density by up to 20 percent compared to the previous generation and up to 40% over competitive cores. The architecture and pipeline are designed to meet the needs of next-generation system-on-chip (SoC) applications and enable the development of a full range of 32-bit processor cores—from low-end, extremely power-efficient embedded cores to very high-performance host solutions that are binary compatible and designed with common pipeline elements. The ARCv2 ISA enables the implementation of complex heterogeneous SoCs with processor cores precisely targeted to meet the specific performance and power requirements for each instance on an SoC, while offering the same software programmer's model to simplify program development and task partitioning.

Features

- 1.81 DMIPS/MHz
- 4.02 CoreMark/MHz
- 2K–32K instruction and data caches (EM6)
- Single cycle access close coupled memory, support for 2-cycle ICCM
- ARCv2 32-bit RISC ISA
- 3-stage pipeline—Harvard architecture
- User-configurable program counter
- Configurable zero overhead loop counter
- Architectural clock gating and enhanced sleep instructions
- IP (Code) protection
- 32-bit instruction and data busses
- ECC/Parity Support
- Integrated watchdog timer
- ARM® AMBA® AHB™ and AHB-Lite™ native bus interfaces
- Big or Little Endian
- Programmable loop counter 8-, 16- or 32-bit

Pipeline

The ARC EM cores have a low-latency 3-stage pipeline that is optimally balanced to achieve very low power consumption with excellent embedded performance. The pipeline is designed to give longer access to memory, allowing maximum clock speeds comparable to typical 5-stage pipelines at all process nodes. The pipeline is based on the Harvard architecture with separate instruction and data memory storage that can be simultaneously accessed. The pipeline supports precise exceptions with a commit point after the second stage.

Configurable Options

The ARC EM processor cores support a broad range of configurable options, enabling optimization for a specific application's performance, power and size requirements. The included ARChitect configuration tool features a graphical interface and produces verified RTL and synthesis scripts that are compatible with industry-standard design flows. With ARChitect, designers can add or remove features that improve the efficiency of the core for their application, including options such as custom instructions, multipliers, hardware divide, memory configuration, program counter width, address bus width, timers, interrupts, register file structure and much more.

Cache Memory for EM6

The ARC EM6 processor supports separate instruction and data L1 cache memory spaces that can be independently configured for 2K, 4K, 8K, 16K or 32K size. The instruction and data cache can be set up by the user at build time to support 1-, 2- or 4-way set associatively, and a line size of 16, 32, 64 or 128 bytes. The caches can be individually configured to support line locking and invalidate, and to offer debug visibility.

Closely Coupled Memory

The ARC EM4 and 6 processors support 512B to 2MB of closely coupled memory (CCM) for both instruction and data memory. For the EM6, the CCM can be used with cache memory to facilitate maximum system performance and flexibility. Both memory spaces can be accessed every clock cycle and both ICCM and DCCM can be read and written to from outside the core through AHB-Lite target interfaces. Both the ICCM and DCCM can be separately configured for 512B, 1KB, 2KB, 4KB, 8KB, 16KB, 32KB, 64KB, 128KB, 256KB, 512KB, 1MB or 2MB.

Register File and Program Counter

The ARC EM4 and EM6 register files are configurable, with a default size of 16 32-bit registers that can be increased to 32 32-bit registers at build time. The register file can be constructed from fast, single cycle access memory or flip-flops, and supports one or two write ports (one is the default) and two read ports. The general purpose registers (r0-r28) can be used for any purpose by the programmer. Some of the core registers have defined special purposes like stack pointers (r28), link registers (r29, - r31) and loop counters. The register file can be expanded to up to a total of 60 registers using the extension core registers (r32 - r59). The ARCv2 16-bit instructions have limited direct access to register r0 - r15 and can indirectly access the remaining registers' various instructions. If an instruction references an unimplemented core register, an Instruction Error exception will be raised. The program counter is read only and located at r63 in the register file. The program counter is a 32-bit word aligned register for use as a source operand in all instructions supporting PC-relative addressing. The default size for the program counter is 16-bit, and this is user configurable at build time to 20-, 24-or 32-bits.

Function	Product	Benefits
Co-Design	nSIM Turbo	• Quickly develop applications with 200 MHz+ speeds
	nSIM	• Fast instruction-accurate and near cycle-accurate simulator for the ARC EM family
	xCAM Generator	• Save six person-months or more of development effort
Software Development	MetaWare Development Toolkit	• Save on hardware memory costs using a compiler that is optimized for smallest code size and speed • Increase productivity with unparalleled hardware and software visibility and profiling
	JTAG Debuggers	• Efficiently debug and bring-up hardware boards • Purchase from world-class vendors like Ashling, Green Hills and Lauterbach
	GNU Tools	• Open source solution optimized for DesignWare ARC IP • Reduce risk with support from Synopsys
Deploy	MQX RTOS	• Extend battery life through Energy PRO power management at the thread level and automatic DVFS • Reduce cost compared to creating scheduler or RTOS from scratch
	Third-Party Operating Systems	• Reuse existing software with DesignWare ARC ports for Express Logic ThreadX and µITRON

Table 1: DesignWare ARC EM4 and EM6 software and development tools

Bus Interfaces

The EM4 and EM6 cores have native support for the ARM® AMBA® AHB™ and AHB-Lite™ bus protocols. This is a build-time option with the AHB interface as the default selection. These enable the solutions to be easily connected to the SoC infrastructure in most chips without incurring any delay or complication in the bus interface.

Multipliers

Optional 16x16 and 32x32 multipliers are available to designers, with the ability to implement one or both at build time. The required number of clocks in the 32x32 multiplier can be configured from 1-9 to complete the multiply, with the default configuration being without a multiplier.

Error Protection

EM cores provides support for error protection and caches where present. The different protection schemes may be combined to achieve several levels of protection against malicious or misbehaving code in critical applications. ARC EM supports two error detection techniques: single-bit error correction, double-bit error detection (SECDED) and parity which detects single-bit errors. Both odd and even parities are supported. Data-only protection or data and address protection are both supported for ECC.

Interrupts and Exceptions

Up to 240 interrupts and exceptions are supported on both the EM4 and EM6. Designers can select any additional number of interrupts up to 240 at build time. The interrupts support multiple user-defined priority levels.

The Exceptions Reset, Memory Error and Instruction Error have a higher priority than the highest priority interrupts. The interrupts are serviced through a jump table that allows higher flexibility in the location and implementation of the interrupt vectors. Interrupts can be triggered by hardware or software.

ARC Processor EXtension (APEX) Technology

The EM processors are designed to be extendable with the addition of user-defined instructions. These extensions may include more core and auxiliary registers, new instructions, and additional condition code tests. The extensions of the core enable efficient addition of proprietary hardware and other capabilities that are tightly coupled to the core and can greatly increase system performance.

Licensable Options

- FPU Floating Point Unit offers single and double precision math instructions
- Enhanced Security Package enables designers to create a tamper-resistant, secure environment to protect systems from vulnerabilities
- CryptoPack provides the ability to speed up software encryption implementations by adding custom instructions and registers using the APEX interface
- Safety enhancement package (SEP) provides hardware safety features and detailed safety related documentation to assist in ISO 26262 ASIL D certification
- The Memory Protection Unit (MPU) gives the software running on the processor core the ability to control access rights to the memory
- The Small Real-time Trace (SmaRT) provides real-time trace features to the DesignWare ARC processors
- ARConnect facilitates multicore integration
- The µDMA controller allows fast DMA transfers with low gate count and low power consumption

Complete Suite of Development Tools

To facilitate rapid development of EM4 and EM6-based SoCs, the cores are supported by a complete suite of development tools. This includes the acclaimed MetaWare Development Kit that generates highly efficient code ideal for deeply embedded applications, the ARC simulators including xCAM and nSIM, and the ARChitect configuration tool.

embARC

The embARC Open Software Platform is an easily-accessible, highly-productive solution for developing software for ARC® processor-based embedded systems and subsystems, especially those targeting the IoT. The comprehensive suite of free and open-source software available from the embARC.org website, including drivers, operating systems and middleware, enables code development to start sooner and complete faster. Documentation and other resources available on the website facilitate the sharing of information and expertise among the ARC-based development community.and expertise among the ARC-based design community.

Documentation

The following documentation is available for the DesignWare ARC EM processor core:

- ARCv2 Programmers Reference
- ARC EM Databook
- ARC EM Integration Guide

Testing, Compliance, and Quality

Verification of the DesignWare ARC EM4 and EM6 processors follows a bottom-up verification methodology from block-level through system-level. Each functional block within the product follows a functional coverage driven test plan. The plan includes testing for ARCv2 ISA compliance as well as state- and control-specific coverage points which have been exercised using constrained pseudo-random environments and a random instruction sequence generator.

Deliverables

The DesignWare ARC EM4 and EM6 processor cores are delivered to system designers as Verilog HDL in the ARChitect IP Library. The HDL is configured and output from the ARChitect IP Configurator tool. To ensure that the product performs as expected, a basic test bench of Customer Confidence Tests (CCT) is delivered with the ARC EM4 and EM6 processor cores.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired interface IP, wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP Prototyping Kits, IP Virtualizer Development Kit and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit synopsys.com/designware.

SYNOPSYS®
Silicon to Software™

01/22/18.CS12064_ARC_EM4-EM6_DS.